System Inductance for MVDC Circuit Breakers

Norbert Doerry
Naval Surface Warfare Center Carderock Division
West Bethesda, MD, USA
Norbert.doerry@navy.mil

John V. Amy Jr.
Naval Surface Warfare Center Philadelphia Division
Philadelphia, PA, USA
John.amy@navy.mil

***Abstract*— One option for implementing circuit protection in Medium Voltage Direct Current (MVDC) naval power systems is to employ Solid-State Circuit Breakers (SSCB) in a manner similar to the employment of conventional circuit breakers in Medium Voltage Alternating Current (MVAC) applications. One important system design characteristic that impacts the operation of SSCBs is the system inductance measured on either side of the SSCB. Because cable resistance is very small, this inductance limits the rate of current rise during a fault. A minimum inductance is required to enable the SSCB to interrupt the fault current within the time needed to detect, localize and isolate the fault. This paper provides a method for approximating the system inductance, offers strategies for increasing it should it prove to be too small, and discusses stability and pulsed load implications.**

***Index Terms*—Circuit Breakers, Fault Location, Fault Protection, Protective Relaying, Switchgear**

I. Introduction

To counter the anti-ship capabilities of potential adversaries, the U.S. Navy is developing high power sensors, high power electronic warfare systems, solid state lasers (SSLs) and electromagnetic railguns (EMRG). While the current state-of-the-market power systems to meet these needs are based on MVAC, MVDC power systems (nominally 6 kV, 12 kV, or 18 kV) are anticipated to affordably power these advanced electric loads with a higher power density. MVDC power system design deviates from MVAC power system design practices in several ways:

- The power system will be regulated entirely by power electronic converters.
- Electric power system dynamics will be faster
- Cable electrical properties will be different
- Due to the lack of a current zero crossing, traditional MVAC circuit breakers will not be capable of interrupting MVDC fault currents.

An alternative to employing MVAC circuit breakers for fault protection is using an MVDC SSCB instead [1][2]. One important system design characteristic that impacts the operation of SSCBs is the system inductance measured on either side of the SSCB [3][4]. This system inductance and the system resistance comprise the Thevenin impedance of the cable system, if the impact of the cable capacitance is ignored (The resonant frequency of the cable is likely to exceed 50 MHz and could be in the gigahertz range for short cables). The system resistance is very small, such that the available fault current can be over ten times the combined current rating of all online sources. For a 120 MW, 12 kV system with a combined current rating of 10 kA, the peak fault current, if allowed to occur, would be greater than 100 kA for all practical cables. A SSCB able to interrupt this amount of current would be unacceptably large and costly.

Consequently, SSCB use a strategy of interrupting the fault current when it exceeds the rated steady-state value, but before it exceeds the fault interrupting capability of the SSCB. In the first microseconds following a bolted fault, the fault current will rise nearly linearly at a rate roughly equal to the system voltage divided by the system inductance. This is a result of the *L/R* time constant of the cable being between 190 and 800 microseconds; in the first microseconds the current has not risen sufficiently for the voltage drop across the resistance to significantly impact the rate of current rise through the inductor. The fault protection relay requires up to several microseconds to detect that a fault has occurred, determine where the fault is, and command the appropriate SSCBs to open. An SSCB in turn, may require fractions of a microsecond to 5 or more microseconds to limit the peak fault current and subsequently bring the current down to zero.

Note that the fast fault clearing speed is an inherent characteristic of the SSCB; the SSCB must be fast in order to interrupt the fault current before it grows larger than the SSCB can safely interrupt. An SSCB that is slower to interrupt will likely cost more because it must interrupt a higher fault current.

II. Minimum System Inductance

The amount of time required to clear a fault will depend on the selection of power electronic devices used in the SSCB. Silicon based devices will generally require more time than SiC based devices. Hence depending on the technology used in the SSCB, the fault current may rise for a period of between 2 and 10 microseconds. The entire interruption period should be less than 200 microseconds (including dissipation of inductive energy in snubbers or Metal Oxide Varistors (MOVs) and recovery of voltage regulation by the sources). Equation (1) describes how to calculate the minimum system inductance. Table 1 provides minimum system inductances

for ranges of time to peak current, multiple of steady-state rated current, and steady-state rated currant.

$$L_{sys\_min} = \frac{1000\, V_{sys}\, t_{int}}{(n_{SSCB\_int} - 1) I_{SSCB\_rate}} \quad (1)$$

L_{sys_min}	minimum system inductance (μH)
V_{sys}	system voltage (kV)
t_{int}	time to peak current (μs)
n_{SSCB_int}	Multiple of steady-state rated current SSCB can interrupt
I_{SSCB_rate}	Steady-state rated current of SSCB (A)

TABLE I. MINIMUM SYSTEM INDUCTANCE FOR 12 KV SYSTEMS

System Voltage (kV)	SSCB current Rating (amps)	SSCB Interrupt Multiple	Interrupt Time (microseconds)	Minum System Inductance (uH)
12	250	2	2	96.0
12	250	5	2	24.0
12	250	10	2	10.7
12	250	2	5	240.0
12	250	5	5	60.0
12	250	10	5	26.7
12	250	2	10	480.0
12	250	5	10	120.0
12	250	10	10	53.3
12	2000	2	2	12.0
12	2000	5	2	3.0
12	2000	10	2	1.3
12	2000	2	5	30.0
12	2000	5	5	7.5
12	2000	10	5	3.3
12	2000	2	10	60.0
12	2000	5	10	15.0
12	2000	10	10	6.7
12	4000	2	2	6.0
12	4000	5	2	1.5
12	4000	10	2	0.7
12	4000	2	5	15.0
12	4000	5	5	3.8
12	4000	10	5	1.7
12	4000	2	10	30.0
12	4000	5	10	7.5
12	4000	10	10	3.3

The minimum system inductance must be compared to the actual system inductance, and if the actual system inductance is too low, a means must be provided to either raise the system inductance, or to modify the SSCB or fault protection relay to enable a lower system inductance.

The peak fault current will also depend on the ability of the sources to limit fault current. Depending on the power electronics topology, the fault current may initially be provided by the output filter capacitors discharging. Once the output filter capacitors are depleted, the peak fault current will be determined by the ability of the power electronics to current limit into the fault.

III. CALCULATING SYSTEM INDUCTANCE

Figure 1 depicts a representative MVDC architecture of a surface combatant based on the reference architecture from Doerry and Amy [5]. The Power Generation Modules (PGMs or generator sets), figure 2, consist of a prime mover (either gas turbine or diesel) a generator with two independent sets of windings, a rectifier for each set of windings, and a grounding and Common Mode (CM) Choke network for each rectifier. Under normal conditions, a fault (either line-to-line or line-to-ground) on either of the two independent windings' grounding and CM Choke network output will not be reflected on the output of the other independent winding's grounding and CM Choke network output. Each of the two independent outputs are connected to one of the two longitudinal MVDC buses (Port or Starboard) via a normally closed disconnect switch. These disconnect switches can be used to isolate the PGM for maintenance, or to reconfigure the power system in the event of damage. The center disconnect switch is normally open and is closed only to reconfigure the power system in the event of damage. The grounding and CM Choke Network is used to establish a ground reference via high resistance ground (roughly 1 megaohm from line to ground) as well as control CM currents.

Figure 3 depicts a notional switchboard employing a SSCB only fault protection system. All sources and loads have a dedicated SSCB as well as the connections to the adjacent zones' switchboards. The switchgear is also anticipated to contain surge suppressors to limit line-to-line and line-to-ground transient voltages. The switchboards will also likely contain the hardware and sensors to implement fault protection relay functions. Not shown are possible connections to an MVDC Casualty Power system.

The PCM-1B in zone 2 is bi-directional in that it can serve as either a load or source. The PCM-1As (one in each zone) may be bi-directional or may be uni-directional.

Table II depicts the number and type of quad conductor cable that can be used for a given breaker ampacity. The differential mode (DM) impedance properties of the cable are also listed as estimated by Doerry [6]. Table III estimates the lengths of each MVDC cable (and the number of paralleled cables) in the example architecture and calculates the cable inductance. The cable lengths are estimated for a moderate size surface combatant, the actual lengths should be considered to vary between 0.5 and 2 times the values estimated.

The system inductance is calculated for each "side" of a SSCB. The sources and cable inductances are converted into a Thevenin equivalent circuit. The Thevenin voltage is approximated as the nominal system voltage. The Thevenin inductance (another name for system inductance) is calculated by first replacing each source with a short, and each load with an open circuit, then calculating the inductance between the positive and negative conductors of the SSCB interface. If SSCBs incorporate an inductor, then that inductance must be incorporated into the calculations. The system inductance will be a minimum when all the sources are online. The system inductance will be a maximum when only one of the sources is online (which one must be determined by either inspection or calculation).

The minimum value of the system inductance for each "side" of the SSCB is used to compare with the required minimum value of the system inductance. If only loads connect to one side of a SSCB, then that side is not a source of fault current and can be ignored. This technique assumes:

- Sources are very stiff in that they likely have relatively large output filter capacitors that can act as a source of fault current and mask any internal inductance of the source.
- Loads are not a source of fault current through design. One way to prevent loads from contributing fault current is to connect them to the MVDC bus via diodes in both the positive and negative conductors.

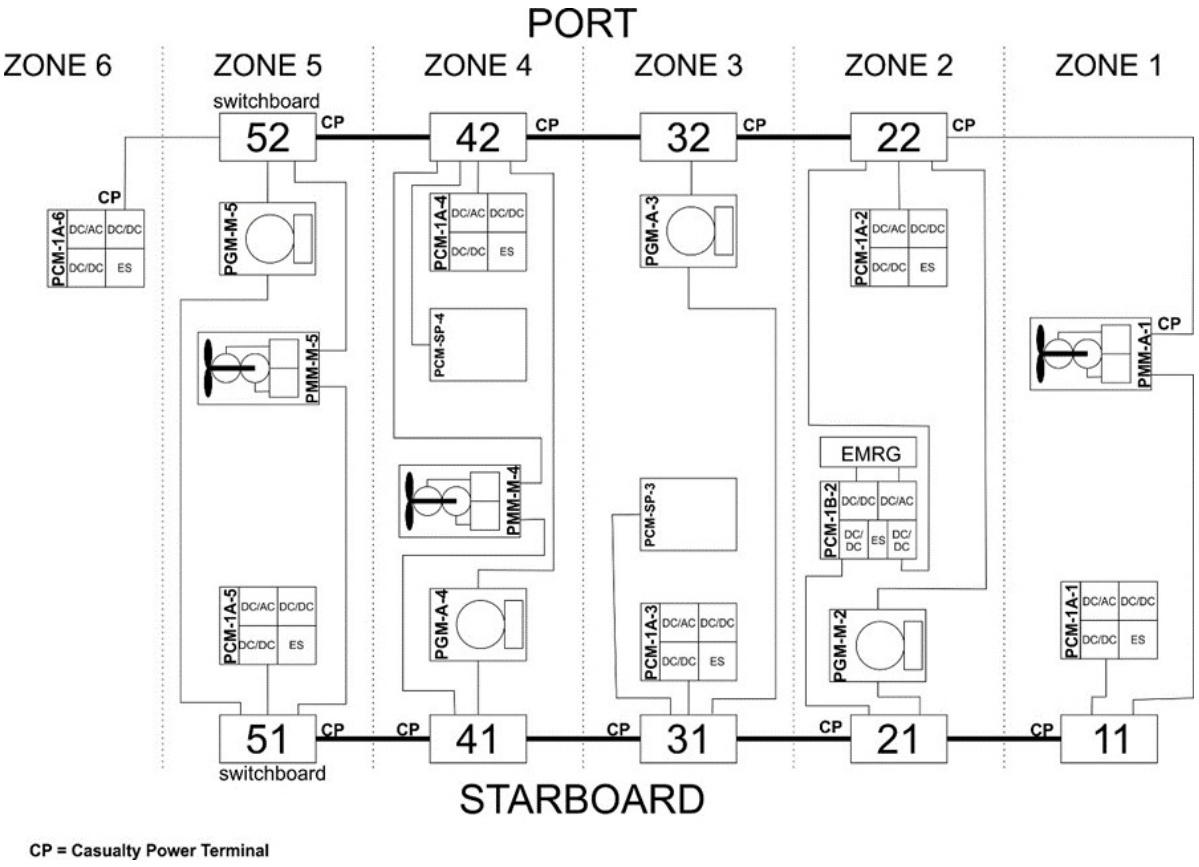

Figure 1. Example systems architecture

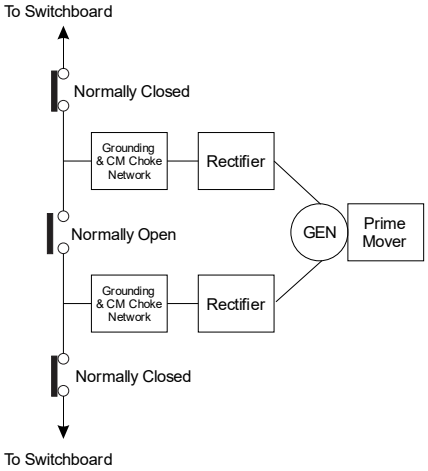

Figure 2. PGM notional architecture

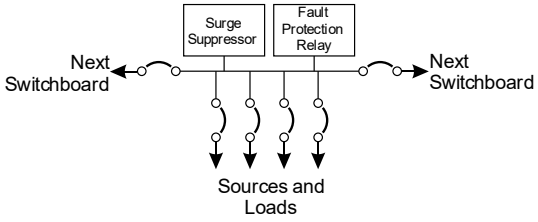

Figure 3. Notional switchboard with circuit breakers

TABLE II. ESTIMATED DM CABLE PROPERTIES (12 KV)

Breaker Ampacity	Cable	Nbr Cables	DM Inductance (one way) uH/1000 ft per cable	DM Inductance (one way) uH/1000 ft per set of cables	DM Capacitance uF/1000ft per cable	DM Capacitance uF/1000ft per set of cables	DM DC resistance (one way) ohms / 1000ft	DM DC resistance (one way) ohms / 1000ft per set of cables
100	SG-50	1	45	45.0	0.046	0.046	0.237	0.237
250	SG-75	1	40.9	40.9	0.054	0.054	0.148	0.148
500	SG-300	1	32.2	32.2	0.088	0.088	0.042	0.042
750	SG-150	2	35.8	17.9	0.07	0.14	0.074	0.037
1000	SG-300	2	32.2	16.1	0.088	0.176	0.042	0.021
1500	SG-300	3	32.2	10.7	0.088	0.264	0.042	0.014
2000	SG-300	4	32.2	8.1	0.088	0.352	0.042	0.0105
2500	SG-300	5	32.2	6.4	0.088	0.44	0.042	0.0084
3000	SG-300	6	32.2	5.4	0.088	0.528	0.042	0.007
3500	SG-300	7	32.2	4.6	0.088	0.616	0.042	0.006
4000	SG-300	8	32.2	4.0	0.088	0.704	0.042	0.00525

TABLE III. REPRESENTATIVE CABLE PROPERTIES FOR EXAMPLE SYSTEMS ARCHITECTURE

From (switchboard)	To (switchboard or equipment)	Ampacity (amps)	Length (f)	one way Inductance uH/1000 ft	set of cables two way Inductance (uH)
11	PCM-1A-1	250	30	40.9	2.45
11	PMM-A-1	500	60	32.2	3.86
11	21	750	100	17.9	3.58
21	PGM-M-2	3500	60	4.6	0.55
21	PCM-1B-2	2000	30	8.1	0.48
21	31	4000	100	4.0	0.81
31	PGM-A-3	500	60	32.2	3.86
31	PCM-1A-3	500	30	32.2	1.93
31	PCM-SP-3	500	30	32.2	1.93
31	41	4000	100	4.0	0.81
41	PGM-A-4	500	60	32.2	3.86
41	PMM-M-4	3500	60	4.6	0.55
41	51	4000	100	4.0	0.81
51	PMM-M-5	3500	60	4.6	0.55
51	PGM-M-5	3500	60	4.6	0.55
51	PCM-1A-5	250	30	40.9	2.45
22	PMM-A-1	500	160	32.2	10.30
22	PGM-M-2	3500	60	4.6	0.55
22	PCM-1A-2	250	30	40.9	2.45
22	PCM-1B-2	2000	30	8.1	0.48
22	32	4000	100	4.0	0.81
32	PGM-A-3	500	60	32.2	3.86
32	42	4000	100	4.0	0.81
42	PCM-1A-4	500	30	32.2	1.93
42	PCM-SP-4	500	30	32.2	1.93
42	PGM-A-4	500	60	32.2	3.86
42	PMM-M-4	3500	60	4.6	0.55
42	52	4000	100	4.0	0.81
52	PMM-M-5	3500	60	4.6	0.55
52	PGM-M-5	3500	60	4.6	0.55
52	PCM-1A-6	250	130	40.9	10.63

The results of these calculations for the example architecture are listed in Table IV for the case where none of the SSCBs have an associated inductor, where all the PGMs are online and assuming that none of the PCM-1As or PCM-1Bs contribute fault current. For this case, the calculated system inductance could vary by a factor of 0.5 to 2 based on the same scaling factor for the range of cable lengths. These calculations indicate that the system inductances for the circuit breakers could vary from 0.2 to 8 microhenries; most are between 0.25 and 2.5 microhenries. In examining Table I, many of the SSCB characteristics, particularly for the lower rated ones, require minimum system inductances above these values. Either a means to reduce the required inductance, or a means to raise the system inductance is needed.

If any of the PCM-1As or if the PCM-1B are able to contribute fault current, then the system inductance will be even lower than those depicted in Table IV.

TABLE IV. SYSTEM INDUCTANCE CALCULATIONS

Switchboard	Cable To	Ampacity (amps)	Cable Inductance (uH)	Side A system Inductance (uH)	Side B system Inductance (uH)	System Inductance (uH)
11	PCM-1A-1	250	2.45	3.98		3.98
11	PMM-A-1	500	3.86	3.98		3.98
11	21	750	3.58	3.98		3.98
21	11	750	3.58	0.40		0.40
21	PGM-M-2	3500	0.55	1.40	0.55	0.55
21	PCM-1B-2	2000	0.48	0.40		0.40
21	31	4000	0.81	1.40	0.55	0.55
31	21	4000	0.81	0.59	1.36	0.59
31	PGM-A-3	500	3.86	0.70	3.86	0.70
31	PCM-1A-3	500	1.93	0.59		0.59
31	PCM-SP-3	500	1.93	0.59		0.59
31	41	4000	0.81	1.45	1.00	1.00
41	31	4000	0.81	0.65	1.81	0.65
41	PGM-A-4	500	3.86	0.78	3.86	0.78
41	PMM-M-4	3500	0.55	0.65		0.65
41	51	4000	0.81	1.36	1.23	1.23
51	41	4000	0.81	0.55	2.04	0.55
51	PMM-M-5	3500	0.55	0.43		0.43
51	PGM-M-5	3500	0.55	2.04	0.55	0.55
51	PCM-1A-5	250	2.45	0.43		0.43
22	PMM-A-1	500	10.30	0.43		0.43
22	PGM-M-2	3500	0.55	2.04	0.55	0.55
22	PCM-1A-2	250	2.45	0.43		0.43
22	PCM-1B-2	2000	0.48	0.43		0.43
22	32	4000	0.81	2.04	0.55	0.55
32	22	4000	0.81	1.23	1.36	1.23
32	PGM-A-3	500	3.86	0.78	3.86	0.78
32	42	4000	0.81	1.81	1.00	1.00
42	32	4000	0.81	1.00	1.81	1.00
42	PCM-1A-4	500	1.93	0.65		0.65
42	PCM-SP-4	500	1.93	0.65		0.65
42	PGM-A-4	500	3.86	0.78	3.86	0.78
42	PMM-M-4	3500	0.55	0.65		0.65
42	52	4000	0.81	1.36	1.23	1.23
52	42	4000	0.81	0.55	2.04	0.55
52	PMM-M-5	3500	0.55	0.43		0.43
52	PGM-M-5	3500	0.55	2.04	0.55	0.55
52	PCM-1A-6	250	10.63	0.43		0.43

IV. OPTIONS TO LOWER REQUIRED SYSTEM INDUCTANCE

Looking at equation (1), there are two ways to lower the required system inductance: Reduce t_{int}, or increase n_{SSCB_int}. Reducing t_{int} can be accomplished several ways.

One way to reduce t_{int} is to command all of the SSCBs to open upon detection of a fault but before the fault has been localized. As soon as the fault has been localized, all the circuit breakers but those needed to isolate the fault are commanded to close. This method may be difficult to successfully implement because the fault localization algorithm must be able to work while all the SSCBs are in the process of opening, or have opened.

Another way is to pick devices that can turn off quickly. Generally, SiC power FETs can turn off much faster than Silicon IGBTs. Other devices are also available.

Increasing n_{SSCB_int} can be accomplished by device selection, or paralleling more devices. This latter method may not be desirable due to the added cost, volume and weight.

V. OPTIONS TO RAISE SYSTEM INDUCTANCE

The system inductance can be raised several ways:

- Each SSCB can include an inductor sized to ensure the minimum system inductance is available for all configurations of the power system.
- Each source can include an inductor sized to ensure that every breaker's system inductance is greater than its required minimum system inductance. An upper bound for this inductance is to take the highest required minimum system inductance of all the breakers and multiply it by the maximum number of sources that can be online at any one time. This multiplication factor accounts for the sources being in parallel.
- If multiple sources are online, then upon detection of a fault, the impacted bus is immediately segmented so that each segment has exactly one source connected to it. This will increase the system inductance while the fault is occurring. Whether this can be done in time to be useful must be determined.

Combinations of the above are also possible.

For systems that rely predominately on SSCBs for fault protection, there will be fewer sources than circuit breakers, so it will likely be less expensive to locate the inductor with the sources. In most cases, since there will be two circuit breakers connected in series between each switchboard, and thus there could potentially be many series inductances between a source and a load, the maximum system inductance for a load will likely be less if the inductance is added at the source. This may be important in ensuring stability.

VI. Fault Detection and Localization Implications

SSCBs that are directly feeding loads need not coordinate with other SSCB; they will trip whenever the current exceeds rated current for more than a specified time, typically a microsecond. Similarly, if a SSCB directly connected to a source is experiencing reverse current, then it too can trip without coordinating with other SSCBs. Source SSCBs without reverse current and all other SSCBs must coordinate to ensure only those SSCBs nearest the fault trip.

Two techniques for fault location are directional protection and differential protection. Both methods may be used at the same time. In both techniques, a zone is established where circuit breakers are installed on each cable crossing the zone boundary. Typically, every switchboard and every cable connecting switchboards are considered a zone. A circuit breaker typically belongs to either one (zone for the switchboard) or two zones (+ zone for cables interconnecting switchboards). In differential protection, for each of the two conductors (positive and negative) the sum of the currents entering the zone is compared to the sum of the currents leaving the zone. If the two are the same, then there is not a fault in that zone. A difference indicates a fault and all the breakers associated with the zone are opened. This method can detect both low and high impedance faults. One challenge with this method is that if the current measurements at the various SSCBs are not taken at the same time, then during a fault when the current rate of change is very high, a false positive for a fault within the zone may be experienced. In directional protection, a fault is sensed if all the SSCBs indicate any non-zero current is entering the zone (positive conductor) or leaving the zone (negative conductor); at least one SSCB must indicate a non-zero current. Directional protection may indicate a false negative if a high impedance (such as an arcing fault) fault is experienced within the zone. The voltage may still be high enough for current to flow in through some interfaces and out on other interfaces. A combination of the two methods is anticipated to result in reliable fault detection and localization. Performing the necessary current measurements, determining whether a fault has occurred using the two techniques, and resolving any disagreement in the results of the two techniques, then command the appropriate SSCBs to open is anticipated to take between 1 and 2 microseconds.

VII. Fault Isolation Implications

Hitachi [7] indicates that silicon medium voltage IGBTs can withstand up to about 6 times rated current for a maximum of 10 microseconds. A sampling of Medium Voltage silicon IGBT module datasheets indicates a maximum turn off time of between 1 and 8 microseconds. Lower voltage (1.2 kV) devices have lower turn-off time while higher voltage (6.5 kV) have higher turn-off times. SiC FET modules have a maximum turn off time between about 0.1 and 1 microseconds.

While the performance of a SSCB will naturally depend on its design, the time to peak fault current will likely fall within the range of 2 to 10 microseconds. The total interruption time will be longer and will depend on the design of the snubber or surge suppressor across the switching device as well as the "stiffness" of the sources. This snubber or surge suppressor prevents the magnitude of voltage spikes to exceed the rating of the switches. The voltage spikes result from the fast turn-off of the fault current interacting with the line inductance. The total duration of the power interruption could be on the order of 100 to 200 microseconds.

VIII. Stability Implications

The stability condition for a constant power load for a source employing a droop characteristic is given by [5]:

$$P_0^2 < \frac{V_B C V_{NL}^3 d(1-d)^2}{L} \tag{2}$$

Where

P_0	Rated Power
V_B	Nominal System Voltage
V_{NL}	No load voltage
d	droop coefficient
C	Load input capacitance
L	System inductance

Equation (2) can be restated as:

$$\frac{C}{L} > \frac{P_0^2}{V_B V_{NL}^3 d(1-d)^2} \tag{3}$$

Hence increasing the maximum system inductance that a load may experience also increases the required load input capacitance to ensure stability. For this reason, it is desirable to only install the minimum extra system inductance needed to ensure the SSCBs can reliably interrupt the fault current. Note that equation (3) presumes the sources and load can implement control algorithms with sufficient bandwidth to ensure its validity. Other control methods are possible which may result in a smaller capacitance requirement.

IX. Pulsed Load Implications

One of the implications of incorporating an inductor with a SSCB that connects with another switchboard is that the inductor will limit how quickly power can be directed from one load (such as propulsion) to a pulse load. To reverse the direction of current through an inductor, a voltage drop is required across that inductor. Since this voltage drop is limited by interface requirements, the current rate of change is also limited based on this voltage drop constraint and the SSCB inductance.

For this reason, it may be beneficial not to install inductors in SSCBs that may experience current reversals when pulsed loads are present. Alternately, the use of a full-wave rectifier to ensure uni-directional current flow through the inductor as described by Ulissi, Lee and Dujic [8] and depicted in figure 4 may be employed. This configuration however, results in extra conduction losses through the diodes. Because the current through the inductor is uni-directional, the use of a physically smaller asymmetric inductor as described by Aguilar and Munk-Nielson [9] is possible.

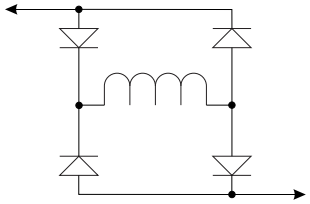

Figure 4. Ensuring uni-directional current flow through an inductor

X. Alternate Fault Detection, Localization, and Isolation Methods

Replacing SSCBs that do not directly connect to a source with a disconnect switch may prove to be more economical. While a disconnect switch can safely conduct rated current indefinitely and fault current for a short time while closed, it cannot interrupt more than a fraction of the rated current. In this hybrid configuration, all the SSCBs open upon detection of a bus fault. Because of the potential for an L/R time constant on the order of 800 microseconds, the fault current may not have decayed sufficiently for the disconnect switches to open for several milliseconds. The SSCB snubbers will decrease this time period somewhat by dissipating the stored energy. During this time period, the fault must be located so that the appropriate disconnect switch can be commanded to open. The appropriate disconnect switches will likely require between 10 and 50 milliseconds to open. It will then take several milliseconds to re-energize the bus. The bus interruption could last between 20 and 60 milliseconds. Loads must be able to accommodate interruptions of this duration.

Another option is to eliminate all SSCBs and rely upon the sources to current limit for a brief period of time to locate the fault, shut down, open appropriate disconnect switches, then re-energize the bus. This option will likely result in bus interruptions longer than 20 to 60 milliseconds.

Another hybrid option is to use a SSCB to immediately partition a faulted bus near its center (between switchboards 31 and 41 or between switchboards 32 and 42). If a source is online in the upfaulted partition, then loads would only see a disruption of less than a millisecond. The faulted portion could see a bus interruption between 20 and 60 milliseconds.

In these alternate methods, the number of SSCBs is minimized. For these cases, installing within each breaker an inductor equal to its minimum system inductance is likely the most cost-effective solution.

XI. Conclusions

The system inductances of the cables in a shipboard system are likely not sufficient to enable fault clearing for a SSCB. Additional inductance must be added. In a fault protection scheme employing only SSCBs, locating the additional inductance with the sources is recommended. In other fault protection schemes where the number of SSCBs is limited, then locating them with the circuit breaker will likely be optimal.

The optimal solution for a particular system will still depend on system design parameters. This paper has demonstrated how to calculate the inductance requirements for a given system design and SSCB design characteristics.

References

[1] C. Pietro, L. Qi, C. Tschida, VR. R. Ramanan, L. Racita, and A. Antoniazzi “High current solid state circuit breaker for dc shipboard power systems,” presented at IEEE ESTS 2019, Arlington VA, Aug 14-16, 2019.

[2] R.M. Cuzner, V. Singh, M. Rashidi, and A. Nasiri, “Converter Topological and Solid State Protective Device Trade-Offs for Future Shipboard MVDC Systems,” presented at IEEE ESTS 2015, Alexandria, VA, June 22-24, 2015.

[3] R Rodrigues, T. Jiang, Y. Du, P. Cairoli, and H. Zheng, “Solid State Circuit Breakers for Shipboard Distribution Systems,” presented at IEEE ESTS 2017, Arlington, VA, August 14-17, 2017.

[4] X. Pei, O. Cwikowski, D. S. Vilchis-Rodriguez, M. Barnes, A. C. Smith and R. Shuttleworth, "A review of technologies for MVDC circuit breakers," IECON 2016 - 42nd Annual Conference of the IEEE Industrial Electronics Society, Florence, 2016, pp. 3799-3805, doi: 10.1109/IECON.2016.7793492.

[5] N. Doerry and J. Amy Jr., "Design considerations for a reference MVDC power system," presented at SNAME Maritime Convention 2016, Bellevue, WA, Nov 1-5, 2016.

[6] N. Doerry, “Impedance of four conductor cable,” Naval Sea Systems Command, SEA 05T Technical Report Ser 05T/011 dated 2 October 2020. Available from http://doerry.org/norbert/papers/papers.htm

[7] Hitachi Power Semiconductor Device, Ltd. (2009) “(High voltage IGBT module) application manual”, NO.IGBT-HI-00002 R2 of Dec 2009. Available from https://www.aepint.nl/wp-content/uploads/2015/05/Application-Manual.pdf

[8] G. Ulissi, S. -Y. Lee and D. Dujic, "Solid-State Bus-Tie Switch for Shipboard Power Distribution Networks," in *IEEE Transactions on*

Transportation Electrification, vol. 6, no. 3, pp. 1253-1264, Sept. 2020, doi: 10.1109/TTE.2020.2996776.

[9] A. R. Aguilar and S. Munk-Nielsen, "Design, Analysis and Simulation of Magnetic Biased Inductors with Saturation-Gap," Proceeding of the 16th Conference on Power Electronics and Applications, EPE'14-ECCE Europe, 26-28 August 2014.
Available from https://doi.org/10.1109/EPE.2014.6910896