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DC Interfaces for Naval Applications

ABSTRACT

MIL-STD-1399-300 and MIL-STD-1399-680 have established a.c. voltage interface requirements for U.S. naval surface ship electrical power systems. Equivalent interface standards have not been established for d.c. interfaces on U.S. naval surface ships. Since future warships are anticipated to have increasing numbers of d.c. interfaces, a working group was established in December 2015 to create new MIL-STD-1399 sections. These standard d.c. interfaces are intended to facilitate the development and integration of d.c. sources, loads, and energy storage. In particular, these interfaces are intended to support emerging electric weapons and high power sensors that have pulse power characteristics exceeding the requirements in the current MIL-STD-1399 sections 300 and 680. In addition to pulse loads, the d.c. interface standards should address stability requirements to ensure system stability when integrated into an overall system, as well as common mode impedance and voltages to limit common mode currents.

This paper describes the current draft standards, summarize feedback from government, industry and academia reviewers, and offers suggestions for addressing the issues that were identified.

INTRODUCTION

The emergence of near-peer competitors to the U.S. Navy has led to the U.S. Navy adopting a distributed lethality approach. As part of this approach, future warships are anticipated to incorporate multiple high power sensors, high power electronic warfare systems, solid state lasers (SSLs), and electromagnetic railguns (EMRGs). This revolution in ship self-defense and offensive capability will enable surface combatants to greatly increase the amount of ordnance each ship can carry, achieve a favorable cost exchange ratio (the cost of shooting down / destroying a target is less than the value of the target) and enable control of seaways where and when needed.

The power systems of our future warships must evolve to the changing power characteristics of the new weapons systems. While a.c. power generation and distribution systems have served the U.S. Navy well for the past eighty years, the anticipated incorporation of multiple high power and pulse loads are anticipated to be more affordably served by d.c. power systems.

To keep current levels to a manageable level (below 4000 amps) power at medium voltage d.c. (MVDC) levels (above 1 kV) will likely be generated and distributed. Notional architectures for a MVDC system are described by Doerry and Amy (2015A, 2015C, and 2016). While there are many potential advantages of employing an MVDC system on future warships, some of the more important reasons are detailed by Doerry and Amy (2016):

- High power, highly dynamic electric mission loads are more easily accommodated with MVDC. Because the speed of the prime mover does not directly affect power quality at the MVDC bus (as is the case with a.c. systems) system electrical energy storage can be minimized by employing the rotational inertia of the generator and power turbine (for a gas turbine) as energy storage.
- An active rectifier and appropriate controls decouple the prime mover speed and rotational angle from the power quality of the bus. In an a.c. system, the rotor angles of all the generators are electrically aligned in the steady-state; large restorative currents flow through the system should a disturbance (such as a pulse load) cause the rotors of multiple paralleled generators to not be in alignment. These large currents flow at the same time the current is desired to serve the

pulse loads. Consequently, an a.c. system must be designed for a large capacity.

- Since the speed of the prime mover is decoupled from power quality on the bus, the generator and rectifier can be optimized for each prime mover without having to incorporate reduction gears or speed increasing gears. The prime mover speed can be varied and controlled to optimize efficiency and/or dynamic responsiveness.
- Power electronics can control fault currents to levels considerably lower than with a.c. systems employing conventional circuit breakers. Lower fault currents reduce damage during faults. Faster fault isolation also minimizes the amount of energy storage loads need to continue operating while the fault is cleared.

A number of mission system loads currently incorporate a considerable amount of power conditioning equipment to produce d.c. power at voltages at or below 1 kV. Discussions with Government and industry engineers have revealed that if the power system provided d.c. power with sufficient power quality and quality of service, then much of the power conditioning equipment within the mission systems could be eliminated. The Navy is currently developing power conversion equipment with associated energy storage to provide the requisite power quality and quality of service. This equipment is generally referred to as an Energy Magazine (NAVSEA 2015) or a PCM-1A (Doerry and Amy 2016).

One of the barriers to implementing d.c. interfaces onboard naval ships is the lack of interface standards. MIL-STD-1399 section 300 (for low voltages) and section 680 (for high voltage) are interface standards for conventional a.c. power systems. Comparable d.c. interface standards do not exist for MVDC or for many of the voltages of interest at or below 1 kV. IEEE Std 1709 does provide guidance for voltages between 1 and 35 kV, but this guidance is not sufficient for ensuring successful integration of equipment developed by multiple manufacturers.

One of the goals of an interface standard is to enable equipment development to occur prior to or concurrent with system development. The interface specification must enable equipment built and tested to the standard to be successfully integrated into an overall system. Furthermore, equipment compliant to the interface and used on one ship should not require modification to be used on another ship. Hence the interface should not depend on specific design details or characteristics of a particular ship power system design.

Doerry and Amy (2015B) provided an initial proposal for the d.c. interfaces to spur discussion. Subsequently, a government team was established to begin the development of new MIL-STD-1399 sections for d.c. voltages above 1 kV and d.c. voltages at or below 1 kV. In November 2016, this team released a Request for Information (RFI) (NAVSEA 2016) to gain industry, academia, and Government feedback on early draft standards. In addition to general feedback, answers to sixteen specific questions were solicited. These sixteen questions are listed in Appendix A.

FORMAT OF DRAFT STANDARDS

Two different draft standards were created. The first defines three standard voltages for medium voltage d.c. power generation and distribution: 6 kV, 12 kV and 18 kV. The voltage levels are based on recommendations from IEEE Std. 1709, a desire to keep generator and main distribution currents below 4000 amps (to avoid thermal issues with switchgear and reduce the weight of distribution cabling), and the availability of power electronics. This standard was given the "working" name MIL-STD-1399-MVDC. The actual designation for this standard will be different when it is eventually approved.

The second standard, given the working name MIL-STD-1399-LVDC, defines standard voltages of 375 volts, 650 volts and 1000 volts. These voltage levels are common with equipment on DDG 1000 and similar to voltages used in a number of systems in development. The 375 volt level is consistent with an industry telecommunications standard (ETSI 2011). Several mission system programs were consulted and validated that their designs could accommodate the three standard voltages while still meeting the objective to reduce power conversion equipment within the mission systems.

Both draft standards have the same format based on MIL-STD-962:

1. Scope
2. Applicable Documents
3. Definitions
4. General Requirements
5. Detailed Requirements
    - 5.1 Electrical Power System Characteristics
    - 5.2 Load Requirements
    - 5.3 Load Verification Methods
    - 5.4 Source Requirements
    - 5.5 Source Verification Methods
6. Notes

One of the differences between these draft standards and MIL-STD-1399 sections 300 and 680 is that the new d.c. standards are proposed to incorporate two interfaces as depicted in Figure 1. One interface defines the distribution equipment to load interface (as was done in the a.c. standards) and the other interface defines the distribution equipment to source interface. The integration of sources and loads and the design of the distribution equipment to meet its interface requirements will be governed by a design practices and criteria (DPC) manual.

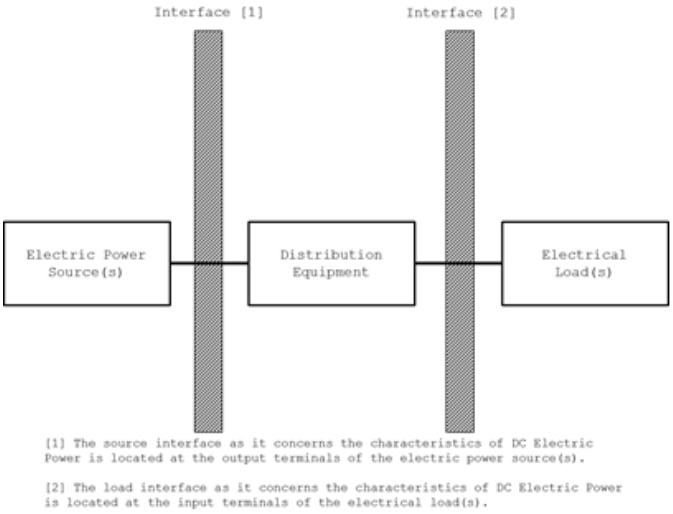

Figure 1: DC interfaces (NAVSEA 2016)

The inclusion of both interfaces is desirable because future power systems will likely incorporate bi-directional power conversion equipment that will at times behave as a load, and at other times behave as a source. Having both sets of interfaces in a single document will help ensure the two sets of interfaces are compatible.

In any standard, a precise definition of terms is critically important. Appendix B provides the definitions used in the draft standards.

Most of the interface requirements are in section 5. The load requirements and the source requirements are in separate sections. Similarly, the verification methods for loads and sources are in separate sections. This was done to avoid confusion as to which requirements and verification methods apply to the sources, and which apply to loads.

A critical subsection of the final section is 6.2 Acquisition Requirements. This subsection provides guidance for the development of acquisition documents that invoke the standard.

MVDC REFERENCE SYSTEM

The draft MVDC standard does not currently incorporate a reference system. Feedback from multiple sources indicate that incorporation of or citation of a reference system to provide context for the interfaces would be of great value. The DPC manual will likely be the proper document to contain this reference system. The MVDC interface standard is being developed with respect to the reference architecture as depicted in Figure 2. This reference architecture has the following salient characteristics:

- All sources and loads connect to the MVDC bus via power electronics. Generators are assumed to have active rectifiers with a switching speed above 1 kHz.
- Bus nodes may be used to isolate sections of the bus, loads, and sources as needed.
- Distributed energy storage provides power continuity to critical loads while faults are cleared on the MVDC bus. (Accomplished by PCM-1A in Figure 2)
- The power system neutral of the MVDC bus will be isolated from the neutral of the in-zone distribution system. (Accomplished by PCM-1A in Figure 2)
- Power electronics of sources and loads limit the magnitude of fault currents.
- PCM-1As may be able to act as shunt active filters to address current ripple.

- Controls ensure loads receive power and energy at an acceptable rate and sources provide the power and energy at an acceptable rate within their capability.

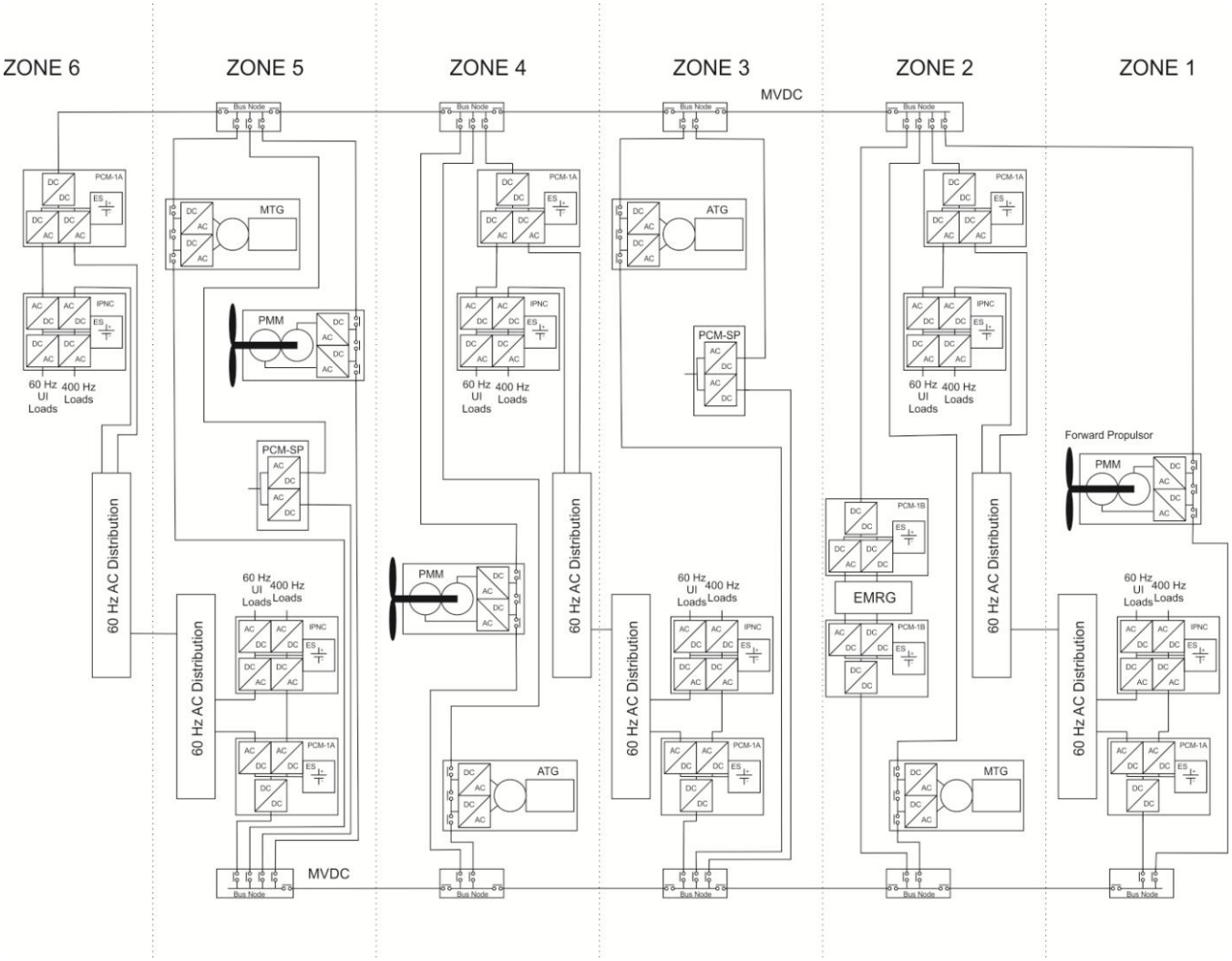

Figure 2: MVDC Reference Architecture

MVDC LOAD INTERFACE CONSIDERATIONS

As expected, feedback from the RFI was not always consistent, but knowing the topics where there is not general agreement is of use in planning future efforts.

General agreement was achieved on the following parameters:

a. **Nominal System Voltage (6 kV, 12 kV, 18 kV)** None of the responses suggested other voltages. These voltages are based on IEEE Std. 1709. One reviewer suggested reducing the allowable voltages to only 12 kV.

b. Worst Case voltage offset from Positive Terminal to Ground and **Worst Case voltage offset from Negative Terminal to Ground.** These parameters are based on what is expected on an unfaulted conductor when the other conductor has a line to ground fault. Continued operation with a line to ground fault is not envisioned. Line to ground faults are anticipated to be detected, localized, and isolated within a relatively short period of time, perhaps under a second.

c. Load behavior during faults. Several reviewers commented that the load behavior to a bus fault should be described. Options include limiting di/dt, minimum inductance, requiring diodes, etc.

Significant discussion was provided on the following parameters

1. **Load maximum steady-state voltage ripple**. Several reviewers stated that the system cost would be minimized by limiting this value to between 1% and 3% (5% as recommended by IEEE Std. 1709 should be the upper bound). They reasoned that the cost to filter the ripple at the source would be cheaper than requiring the input power conditioning of the loads to accommodate a larger voltage ripple The added capacitance for the filter would improve stability as well. Fast semiconductors at the sources can prevent the capacitors from discharging during a fault.

   Other reviewers noted that loads could help limit the voltage ripple by controlling their current ripple through the manner in which they are designed and operated.

   One response stated that the ripple frequency used in the verification method, specified as 1 kHz, was too low; use of high speed generators or other types of power electronics could increase this frequency to between 1.5 kHz and 5 kHz. 1 kHz was chosen as a not too conservative "worst case" condition. Note that the loads may be designed and qualified prior to the design of the generator set. The verification method does allow for acquisition documentation to specify a different ripple frequency.

2. **Load Voltage Transient Tolerance and Load voltage transient recovery time**. Some considered 10% reasonable for load step changes. Others preferred a smaller value on the order of 5% for load step changes. If the transient tolerance is reduced to 5%, then a recovery time of 100 ms or longer is acceptable. One reviewer commented that the load voltage transient tolerance should account for voltage ringing due to extremely fast fault isolation or vacuum breaker current chopping. The transient could be up to 2 times the nominal system voltage, but for a very short duration (likely on the order of a millisecond). If snubbers are required in the distribution system, the transient will be considerably less.
   Other reviewers suggested that pulses be considered a transient and recommended examining larger values than specified.
3. **Load Voltage Interruption Tolerance Time.** This parameter depends on the method for fault detection, localization, and isolation. One response indicated that the interruption tolerance times needs to be much greater than 20 ms in a breakerless approach (some have suggested several seconds while other studies suggest between 65 and 100 ms) and could be less than 5 ms if fast fault clearing is implemented.
   One reviewer observed that the load voltage interruption tolerance time should include the time to clear a fault, the duration of current inrush of loads, and the transient response time of the sources.
   The expected performance of loads to the voltage interruption is also important. The three loads envisioned for the MVDC system, Propulsion Motor, PCM-1A, and large combat systems load (such as a railgun) must have their performance defined during the voltage interruption (probably incorporated as part of acquisition requirements in section 6.2 and /or clarified to a greater extend in section 5.2.2). The PCM-1A should have sufficient energy storage to continue supplying its load without interruption. The propulsion motor and large combat system loads will likely go into a standby state until power is restored.
   Another reviewer suggested the definition for load voltage interruption tolerance time be clarified. In particular, a power interruption should be defined to occur whenever the bus voltage is in the load abnormal service steady state voltage range and also not within the limits of the voltage transient tolerance.
   One reviewer commented that the verification method was too simplistic. The test should consider shorting the conductors to the unit under test during the interruption to simulate a line to line fault that could discharge the input capacitors of the load. Consideration should

also be given to specifying the voltage rate of change at the end of the interruption. Should the Load Maximum inrush Current or Load Maximum current rate of change limits apply following an interruption?

One reviewer suggested a graph be provided for the frequency of voltage interruptions (number of interruptions per unit time) as a function of voltage interruption duration.

4. **Voltage Spike Waveform.** One reviewer noted that the principal sources of differential mode spikes were fuse clearing and breaker opening. The principal sources of common mode spikes are ground faults or lightning strikes. Systems that share grounds will likely share common mode spikes. Isolating ground systems is a useful technique for limiting the impact of common mode grounds. The reviewer recommended addressing each source of spike independently.

   Consideration should be given to separately addressing Basic Impulse Level (BIL) and voltage spikes. BIL is usually intended to account for lightning strikes of terrestrial power systems. Since it is unlikely that power conductors on a ship will be directly impacted by lightning, the associated spikes will most likely be capacitively coupled. BIL is generally applied to insulation systems at a voltage above that for which arrestors are designed to limit. Voltage spikes typically use the same waveform, but account for voltages resulting from switching of inductive elements. Voltage spikes are applied both line to line and line to ground. One comment was to have the waveform "squared off" and extended in duration. The voltage spike amplitude specified (2500 volts) was evaluated by one reviewer as a bit high, but doable; a voltage of spike of equal magnitude to the nominal voltage would be too high.

   IEEE Std. 1709 recommends a rated lightning impulse withstand voltage for line to ground with a peak value of 75 kV for a 6 kV system, 95 kV for a 12 kV system, and 110 kV for an 18 kV system. These levels are not applied line to line. Whether these values are appropriate or cost drivers (both in equipment design and test execution) needs further investigation. Thoughtful design of common mode chokes and grounding systems within the sources and loads may enable meeting these requirements at relatively low cost.

   IEEE Std. 1709 also provides a rated short duration withstand voltage to ground for 1 minute that is only intended to be applied to cable, fuses, switches, and bus work (not to semi-conductors) as a test of the insulation system. This rated short duration withstand voltage is consistent with the test method standard detailed in MIL-STD-202-301. As this is a test of the insulation system, it is not clear that this should be part of the interface standard; there is no expectation that the condition described in the test will be observed in operation.

   Concern was also expressed with the ability to conduct the spike tests at full power. The BIL testing is usually not conducted while the equipment is operating. Equipment must be running for the spike test. Being able to inject the spike at the required voltages and power levels while the equipment is operating could require very expensive test equipment. Assuming that spikes occur primarily due to switching events, the frequency of spikes will likely be much less than the specified 4 times an hour. All of the loads are controlled; they normally would not be turned off by abruptly shutting off their power.

   One reviewer suggested the figure describing the spike should be part of the definition. The waveform depicted however, is a specific spike waveform to be used for testing and is therefore a requirement.

5. **Load Maximum Current Ripple** and **Load Maximum current ripple frequency limits.** Several reviewers questioned the applicability of MIL-STD-461 CE101 frequency limits; noting that this standard is intended for equipment of much lower power levels.

One reviewer suggested that the maximum current ripple be a multiple of the voltage ripple. Note that for a resistive load, the current ripple as a percentage of steady-state current will be the same as the voltage ripple as a percentage of steady-state voltage.

Another reviewer stated the CE101 frequency limits should apply, but only in the steady-state. The limits should not apply during transients or pulses. Others noted that the CE101 limits start at 30 Hz, the standard may need to extend the limit down to 10 Hz or lower.

Minimizing ripple to minimize EMI was discussed by several reviewers.

Another suggested using the power ripple filtering plot depicted by figure 3 of Temkin et al. (2016). This plot however, does not apply to the pulse load directly, but to the required level of filtering by an active filter. It could apply to the input of a PCM-1A where the PCM-1A provides the functionality of an active filter.

6. **Load Maximum inrush Current.** One reviewer recommended that inrush current be limited to 100% of rated current. Others recommended that the load maximum current rate of change not apply during startup to avoid having to include inductors and rely only on resistors for pre-charging capacitors. On the other hand, the need for a common mode choke to control common mode current may provide an inexpensive means of providing a differential mode impedance suitable for limiting inrush current.

   Another reviewer recommended establishing different conditions for energizing a de-energized bus (when precharge circuits are engaged) and following a short term interruption (when precharge circuits are not engage). This reviewer recommended that the load maximum inrush current be a function of the rated power of the device to preclude smaller devices from having pre-charge circuits. The duration of the inrush should also be limited.

7. **Load Maximum pulse load.** A reviewer expressed concern that a pulse load could result in a source being overloaded. This issue requires clarification, either within this standard, or within the DPC manual. A source should never be required to operate outside the bounds of the source requirements listed in section 5.4; the distribution system and controls should preclude a source from having to provide more than its rated power. The source maximum steady state current limit is the current overload requirement.

   Another reviewer suggested the pulse requirements be defined in terms of frequency. Assign responsibility for low frequency components to prime mover based sources, and high frequency components to energy storage within the power system, and energy storage within the loads.

   Another reviewer suggested that MW/s rather than A/s was a more appropriate measure for pulse loads.

8. **Mission Critical Equipment.** A question was asked if there would be anything connected to the MVDC bus that was not mission critical equipment (MCE). While it would not be unusual for all loads on the MVDC bus to be MCE, there may be applications in the future where this is not the case. Furthermore, depending on requirements, only a portion of the propulsion load may be considered MCE. One may not be required to operate at maximum speed under emergency conditions.

9. **Grounding and common mode impedance.** Several reviewers recommended that grounding and common mode impedances should be better defined and specified. Several reviewers recommended high impedance grounding to limit ground currents. Ongoing work suggests that the input to all sources and loads provide a high d.c. resistance and low common mode impedance to ground and a common mode choke to limit common mode currents across the interfaces. Within source and load boundaries (i.e. Propulsion motor and associated drive), the common mode current should be less than about 3 to 20 amps (based on ground current limits generally applied to high impedance grounded a.c. systems). Large power equipment will have

large parasitic capacitances to ground; efforts to limit the common mode voltage can be expensive if the allowable common mode current value is set too low. Across the interface, the common mode current should be less than about 0.5 to 1 amp to limit EMI and coupling of common mode circuits with other equipment. The d.c. resistance from each conductor to ground should be very high (> 100 kilo-ohm) to limit the steady state d.c. losses while still allowing for balancing resistors to establish the d.c. ground reference. There is a general consensus that the 30 mA in section 5.2.3 is too low.

10. **Human Body Leakage Current.** Reviewers commented that conducting the associated test with the unit under test ungrounded was impractical and likely dangerous. The test, if conducted, should be conducted with the equipment properly grounded.
11. **Modeling and Simulation.** A desire was expressed for using modeling and simulation for validation that requirements would be met in lieu of specific at-power testing.
12. **Current Ratings**. One reviewer recommended identifying maximum current ratings for the different voltage levels. Note that a given ship will likely only incorporate one of the MVDC voltages, the selection of that voltage will depend on current ratings of available devices. This discussion is probably best contained in the DPC manual.

MVDC SOURCE INTERFACE CONSIDERATIONS

General agreement was achieved on the following parameters:

a. **Nominal System Voltage (6 kV, 12 kV, 18 kV)** None of the responses suggested other voltages.
b. Source steady-state voltage range: 0 to rated power
c. Worst Case voltage offset from Positive Terminal to Ground and **Worst Case voltage offset from Negative Terminal to Ground**.

Significant discussion was provided on the following parameters

1. **Source steady-state voltage tolerance**. Some responses indicated that the system cost would be minimized by keeping this value below 1% because the cost of centralizing filters at the sources is likely cheaper than distributing the filters among the loads. Others preferred this parameter be in the 2% to 5% range to limit the size of filters at the sources. It is not clear if the responses considered that steady-state values are proposed to be calculated based on a 100 ms moving time window (section 4.6 of the draft standard) which results in frequencies substantially below 10 Hz being reflected in the steady-state values. The active rectifiers of generators should be capable of responding to deviations in the steady-state value within milliseconds. The size of the filters would be impacted greater by the voltage ripple requirements. If voltage droop is used as part of a power sharing scheme among paralleled generators, a smaller value would be preferred to avoid power being unequally shared.
When using a voltage droop method, the commanded reference voltage at the beginning of a time window would be based on the steady-state current of the previous time window.
The definition for the source steady-state voltage tolerance should be clarified to account for a changing commanded reference voltage during a sampling time window. Even though a commanded reference voltage would occur at the beginning of a time window, time windows overlap so that the change in commanded reference voltage would also occur in the middle of a different time window.
2. **Source Steady-State voltage ripple.** Ripple is measured with respect to the steady-state voltage over a 100 ms window. Consequently, the ripple calculation attenuates frequencies appreciably lower than 10 Hz. Several reviewers did indicate a need to separate the slow requirements that the generator and prime mover could handle (steady-state) and those that would require bus capacitance or other methods

to address. A general desire to keep the steady-state voltage ripple small (closer to 3.5% as compared to 10%) based on the assumption that a large voltage ripple provided by the source will result in an increase in the current ripple. The definition of the source steady-state voltage ripple does not accurately reflect voltage ripple when the commanded reference voltage changes during a sampling time window.
Differentiating between lower frequency ripple , perhaps intermediate frequencies, and higher frequency noise was also suggested.
One reviewer suggested it may be desirable to provide a ripple requirement as a function of frequency for loads with no ripple current (or for the no-load condition). Another option would be defining the ripple requirement for a resistive load (which would simplify verification).

3. **Source Voltage Transient Tolerance and Source Voltage Transient Recovery Time**.
From the discussion provided by reviewers, differentiating among transients, pulse loads, and ripple can be difficult. The definition of a transient discusses sudden application or removal of a load, but does not discuss how this differs from a pulse. Because the proposed transient is of equal or shorter duration as the sample window, it may be desirable to replace the Source Voltage Transient Tolerance and Source Voltage Transient Recovery Time with a parameter for Source Peak Voltage Ripple. The voltage ripple is defined as an rms value, also defining a peak value would cover the transient conditions in addition to pulse loads.
MIL-STD-704 specifies electric power interfaces for aircraft. It defines ripple in terms of "Distortion" and "Ripple Amplitude" Distortion is the rms value of the alternating voltage component on the d.c. voltage and ripple amplitude is the maximum absolute value of the difference between the steady-state and the instantaneous d.c. voltage.
In a preliminary review of the draft standard a reviewer noted that the source transient tolerance test is insufficient for ensuring a source can stably support a pulsed load. The draft standard was modified to explicitly require the programmable load to regulate to a commanded power.

4. **Source Maximum Current Ripple.** If PCM-1As are capable of acting as shunt active filters, or other shunt active filters are included to address the current ripple, then this requirement can be 3% to 5%. If shunt active filters are not included in the design, then the source requirement should match the load requirement.
5. **Resistive Load Banks vice Programmable Loads.** A desire was conveyed to use simple resistive load banks for testing instead of more expensive programmable loads. It was noted that using Power Hardware in the Loop testing could add considerable cost to equipment testing.
6. **Verification Methods.** One reviewer stated that industry should have the equipment, and if not, a test service could be hired.
Additional information was desired on the spike generator and its application to d.c. equipment.
7. **Source Current Limit Test.** The need for the temperature to stabilize during the test was questioned. The voltage during the constant current range would occur during an abnormal condition that would not be expected to last a long time.
8. **Temperature Stability Criteria.** Relaxing the criteria to 2 degrees Celsius in 30 minutes would better account for chamber variation and measurement error. Also, with large equipment, achieving thermal equilibrium for all tests could take a significant amount of time and result in high testing costs.
9. **Stability**. Establishing stability criteria was recognized by several reviewers, but developing a generalized method independent of specific system designs was viewed as a challenge. In particular, sources and loads may have very different development schedules. Some expressed a desire for vendors to provide dynamic models so that system stability could be assessed. Others indicated that provisions should be made to add additional capacitance as necessary to stabilize the constant power loads.

For small signal stability it was observed that at low frequencies, system stability is dominated by load and source controls. At high frequencies, input and output filter dynamics have the greatest impact on system stability.

Providing the source controllers with higher bandwidth than the loads can aid in maintaining small signal stability.

There are multiple methods for defining acceptable operating points to avoid small signal stability. One reviewer suggested that the standard specify the criteria to use.

If the sources and their impedances in a system were known first (or specified), one reviewer references a closed-form method for establishing load impedance specifications. (Feng et al. 1999 and 2002) This reviewer suggested standardizing design and analysis methodologies and parameters rather than unilateral restrictions. While the reviewer suggested these methodologies be incorporated into the Electrical Power System Characteristics (5.1) section, the DPC is likely a more appropriate place for these methodologies.

For large signal stability, a need was expressed for ensuring the transient limits were coordinated with the stability approach.

One option expressed was to specify damping factors for eigenvalues as a function of frequency when a source supplies a constant power load via a cable of fixed length. Could be evaluated via simulation of validated models.

10. **Additional Source Requirements**. Methods for load sharing and current ripple sharing among paralleled sources (such as droop) should be addressed either in this standard or elsewhere. Voltage restoration by a source after a fault should also be discussed. The requirement for sources to be voltage-source converters should be explicitly made. More discussion is required for the source maximum steady-state current limit as it applies to the source steady-state voltage range: constant current. In particular the performance requirements on the current regulation should be specified.
11. **Need for source requirements**. One reviewer suggested that only load requirements be specified; use equipment specifications for sources to define the source requirements. This however, would require multiple standards and specification to be coordinated over time, which could be very challenging.
12. **Voltage drop in distribution system.** One reviewer recommended explicitly stating the assumptions for voltage drop in the distribution system.
13. **Diagrams.** One reviewer recommended including diagrams to supplement definitions
14. **Energy Storage.** One reviewer indicated that the document does not provide enough guidance on energy storage. In particular the transition from acting as source to a load and vice versa needs better definition.
15. **Synergy by adding bus capacitance and ultrafast fault protection.** One reviewer noted that employing significant capacitance in the bus can solve many EMI, ripple, stability, and other challenges, but at the expense of potentially higher fault currents. Ultrafast fault protection, which can isolate faults in several microseconds, limit the fault currents to very low levels.
16. **Definition of Load maximum current rate of change and load maximum pulse load.** One reviewer questioned the need for having to sample the current waveform at the specified rate. The rate specified is intended to measure for compliance and need not be measured during operation if the load is guaranteed not to exceed the rate. Reviewer recommended a graphic be provided and interpreted the definition to be a requirement. It may be appropriate to provide the specifics of the measurement in section 4.
17. **Definition of Source steady-state voltage range**. One reviewer questioned the inclusion of "constant power mode" in the definition. The steady-state voltage range is intended to apply for two regulation modes: droop, and constant power. The definition should be clarified that droop and constant power are not occurring at

the same time. Review comments also indicated a need for a better definition and description of different regulation modes of sources.

LVDC REFERENCE SYSTEM

Similar to the MVDC interface standard, reviewers expressed a desire for a better understanding of the system context for the LVDC system. Figure 3 depicts a notional architecture for a PCM-1A as depicted in Figure 2 and for the "Energy Magazine" as envisioned for back-fit and modified repeat applications. For Energy Magazine applications, the input modules (I-Modules) are anticipated to have a three phase 60 Hz. a.c. interface in accordance with MIL-STD-1399-300 or MIL-STD-1399-680. For PCM-1A applications the I-Modules will have a MVDC interface in accordance with the MIL-STD-1399 MVDC interface described above. The set of available energy storage modules (ESM) and output modules are anticipated to be the same. Large loads will likely have dedicated O-modules. Smaller loads will likely employ a traditional radial distribution from common O-modules and fast circuit protection to isolate faulted feeder cables and equipment. The Integrated Power Management Center (IPMC) procured to MIL-PRF-32272A has the ability to provide no-break transfer between multiple sources and can provide both a.c. and d.c. power at a variety of voltages including those proposed for MIL-STD-1399-LVDC.

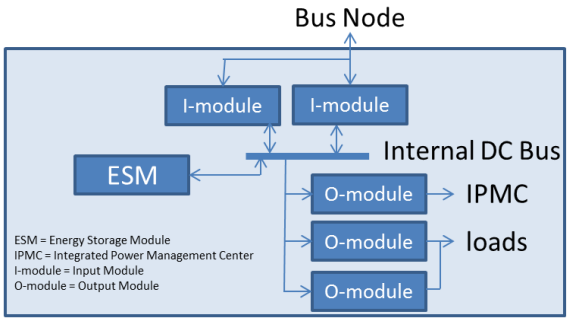

Figure 3 PCM-1A or Energy Magazine architecture

LVDC INTERFACE CONSIDERATIONS

Many of the comments for the MVDC interfaces also apply to the LVDC interface. The differences in the reference systems however, do result in several differing considerations.

a. **Context of Type 1 and Type 2 Power**. For the 1000 volt interface, two types of power are listed. Type 2 has a larger normal service steady state voltage range, but allows pulses with higher current ramp rates. Type 1 power would be conditioned within the PCM-1A or Energy Magazine. Type 2 power would likely be connected only via fault protection to the internal bus and energy storage of the PCM-1A or Energy Magazine. This context should be provided or referenced in the standard.

b. **Nominal system voltage**. One reviewer suggested the Navy only support 1 kV. Another reviewer suggested adding 540 volts and 725 volts as nominal system voltages.

c. **Load normal service steady voltage range**. One reviewer suggested adjusting the lower limit to 85% for the 850 volt interface to support one particular weapon system. Also suggested adjusting the lower limit for the 1000 volt Type 1 interface to 94% for another particular weapon system.

d. **Load voltage transient interruption time**. This parameter should not apply for loads directly connected to dedicated output modules of a PCM-1A, Energy Magazine, or IPMC. This parameter accounts for the amount of time needed to clear a fault. Fault clearing time on a dedicated connection has no significance.
In the case of multiple loads powered by the same output modules, high speed fault clearing is desirable and achievable. From comments received (and other research) fault clearing time below 10 ms should be achievable. The applicability of the load voltage transient interruption time should be specified in the acquisition requirements (section 6.2). The DPC should provide guidance for when mission critical equipment should be provided power from dedicated output modules. (Guidance could be MCE with a rated load current of 20 amps or greater, or loads characterized as pulse loads).
One reviewer stated that the load voltage interruption tolerance time could be longer because any load that was sensitive to an

interruption should be provided an uninterruptible power supply (UPS). This however, is contrary to one of the affordability goals to minimize the need for individual loads to require UPSs.

Another reviewer suggested using the 70 ms and 2 seconds from MIL-STD-1399-300B. However, these parameters are based on performance of a.c. automatic bus transfer devices and circuit breakers.

e. **Load maximum current ripple.** One reviewer stated the load maximum current ripple should be less than 10%. Another recommended a 10% limit but stated that up to 20% may be acceptable. In any case the PCM-1A, or Energy Magazine must have sufficient energy storage capable of providing the ripple current without exceeding the current ripple requirements on the MVDC (PCM-1A) or a.c. bus (Energy Magazine).

f. **Pulse loads.** One reviewer questioned the need for Load maximum pulse load (control negotiation) and Load maximum current rate of change (control negotiation). The reviewer noted that the upper bound should be determined as part of the control negotiations and not limited.

Another reviewer suggested the description of a pulse should be more fully described and suggested using the nomenclature defined by Doerry and Amy (2015C).

Another reviewer questioned the definition of the load maximum pulse load (section 3.8). Stated it should be the highest peak load, and not the highest of the average of 5 ms sub-windows. The use of an average over a sub-window is intended to filter high frequency ringing.

Another reviewer observed that the source maximum current rate of change (no control negotiation) should be several times greater than for the load to account for multiple loads pulsing at the same time.

g. **Load maximum current rate of change**. Reviewers did not agree on the load maximum current rate of change values. One reviewer stated that the 63 A / ms (no control negotiation) and 125 A / ms (control negotiation) were too high because energy storage in the PCM-1A / Energy Magazine would need to have the full power rating of the load since the sources would not be able to sustain this ramp rate. Another reviewer noted that power electronics should be capable of supporting ramp rates two orders of magnitude greater. One reviewer suggested the limit be based on the rated power capacity of the power system; this would however force a dependency of the load on the power system design and could result in rework should the load be designed prior to the power system.

h. **EMI**. One reviewer stated that EMI for power systems with high frequency switching with wide band gap devices is not adequately covered in MIL-STD-461. In particular the frequency range of CE102 needs to be expanded.

i. **Custom Power**. One reviewer noted that the modular nature of the Energy Magazine, PCM-1A, and IPMC enables custom output modules be developed to meet the needs of specific loads. Therefore, the need for standard interfaces is much reduced.

j. **Voltage Spike Waveform**. A reviewer noticed that the peak voltage of the voltage spike waveform for the sources and loads did not match and recommended that they be the same

FUTURE WORK

The extensive feedback from the RFI indicated continued discussion among Government engineers, academia, warfare systems developers, power system developers, and EMI engineers is warranted to address the issues highlighted above and in the RFI questions detailed in Appendix A.

Government-industry-academia forums targeted to addressing these issues would be of great value in the further development of these standards. Modeling and Simulation efforts would be useful in evaluating different candidate approaches to establishing standards.

CONCLUSION

The introduction of d.c. systems into the fleet calls for a well thought out set of interface standards to promote the ability to integrate advanced power systems with combat

systems. This paper highlights many of the diverse views on the content of these standard interfaces and illustrates area where further discussion and research is warranted.

ACKNOWLEDGEMENTS

The efforts of the many Government, industry and academic contributors participating in the creation of the draft standards and reviewing the RFI are greatly appreciated.

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Appendix A: Extract from RFI

The Naval Sea Systems Command is hereby issuing a Request for Information (RFI) on behalf of SEA 05 (Naval Systems Engineering Directorate) and PMS 320 (the Electric Ships Office) seeking information from electrical equipment manufacturers, systems integrators, academia, and other interested parties to support the development of electrical interface standards for DC power systems applicable to naval warships. The Navy has developed two draft standards and desires recommendations addressing specific issues within the draft standards as well as more general comments as appropriate. The two draft standards are referred to in this RFI as MIL-STD-1399-LVDC for 375 volt direct current (VDC), 650 VDC, and 1000 VDC interfaces; and as MIL-STD-1399-MVDC for 6,000 VDC, 12,000 VDC and 18,000 VDC interfaces. These draft standards are available as attachments to this RFI. The development of these interface standards is in direct support of the Naval Power and Energy Systems Technology Development Roadmap (available from http://www.navsea.navy.mil).

MIL-STD-1399-LVDC and MIL-STD-1399-MVDC will have different designations when issued. Initially, the two documents will likely be issued as Project-Peculiar Documents (PPDs) for specific acquisitions including procurements for a potential Integrated Power and Energy System (IPES) Advanced Development Model (ADM). Once lessons are learned from these acquisitions and are incorporated, the two documents are intended to be new sections of MIL-STD-1399.

The MVDC and LVDC interface standards are intended for future shipboard power systems similar to the power system described in "The Road to MVDC," Presented at ASNE Intelligent Ships Symposium 2015, Philadelphia PA, May-20-21, 2015, attached to this announcement

The LVDC interface standard is also intended for back-fit and modified repeat designs through the implementation of the Energy Magazine as described in the Naval Power and Energy Systems Technology Development Roadmap.

RESPONSES:

While feedback on any aspect of the two standards is desired, responses to the following issues are of particular interest to the Navy:

1. The two draft standards include a number of "TBD"s (To be determined). The values provided alongside the TBD are either a single value or a range of values that the Navy is considering for the particular parameter. Recommendations and rationale for specifying a value for the parameter are desired. (Recommendations need not be limited to the values shown).

2. A number of the parameters and values depend on the eventually chosen grounding scheme for each of the interfaces. Recommendations and rationale for the inclusion or deletion of specific parameters, and the associated value, are desired for various possible grounding schemes.

3. A number of the parameters reflect a balance in increasing cost and complexity of sources vs cost and complexity of loads. Recommendations and rationale for parameters and parameter values are desired based on this balance of impact on sources and loads.

4. The voltage spike waveform requirements are not well understood. Insight into the nature, magnitude, and frequency of spikes on DC distribution systems is sought. Insight on the appropriateness of the proposed requirements is desired. Is the cited pulse waveform appropriate?

5. Only a framework for supporting pulse loads is provided. Recommendations for how the control negotiations should be performed are desired. Also desire feedback on the choice of the pulse load parameters. (i.e. should pulse limits be described in terms of MW/s or A/ms?)

6. The load voltage interruption tolerance time is a balance between the cost and capabilities of fault detection, localization, and isolation within the distribution system, and the holdup time designed into individual loads. Perspective on this trade-off, recommendation for a specific value, and the rationale are desired.

7. An assessment of the practicality, cost, safety, effectiveness, and appropriateness of the different verification methods is desired. Can the intent of these verification methods be captured in less costly methods? Would the acquisition of necessary test equipment be an undue burden on industry?

8. Stability is not currently addressed. Recommendations for parameters (and values) for the interfaces to ensure small-signal and large-signal stability are desired.

9. Recommendations for adding requirements that are missing from the standards are desired.

10. Recommendations for deleting requirements from the standards are desired.

11. The draft standards include requirements for both sources and loads, primarily because certain equipment may at times behave as sources, and at other times as loads (e.g. energy storage, and regenerative loads). MIL-STD-1399-300 only provides the requirements for loads. What are your thoughts on the need to include requirements for sources?

12. Tables 3 and 4 include both "independent" (such as voltage parameters for loads) and "dependent" parameters (such as current parameters for loads). Would you prefer to see these independent and dependent variables listed in separate tables?

13. The current ripple frequency limits as presented are based on MIL-STD-461 CE 101 limits. These limits may prove over-restrictive for pulse load applications. Are frequency limits necessary? If so, should the CE 101 limits be relaxed? How should the ripple frequency limits, if provided, be made consistent with the ability to meet other EMI requirements?

14. Should there be a sentence somewhere describing what Type 2 is (i.e. energy storage floating bus) or is it intended that it is understood based on the values in the table.

15. Should there be a requirement for loads to not provide reverse current into the DC Bus, particularly during faults?

16. Should different parameters from those provided be used? If so, propose the parameter definitions and recommended values for the parameters (i.e. specify line to ground capacitance instead of the current in the capacitor)

Appendix B: Definitions

Commanded reference voltage: The voltage set point a source is regulating the output to. This set point is often a function of the steady-state current in the form of a droop characteristic.

Load abnormal service steady state voltage range: The range of steady state DC voltage that when applied to loads (with voltage ripple ranging from 0 to the source maximum steady state voltage ripple) the loads are not damaged. Loads may lose functionality as long as the loss of functionality does not directly result in damage to other equipment or injury to personnel.

Load maximum current rate of change (control negotiation): The maximum rate of change of the current waveform for a load that can be negotiated between the load and the electric plant control system. The rate of change is calculated using the same method as for the "load maximum current rate of change (no control negotiation)."

Load maximum current rate of change (no control negotiation): The maximum rate of change of the current waveform for a load if a larger value has not been pre-negotiated between the load and the electric plant control system. The change is calculated as the difference between the average value of the current measurements over the first half of a window and the average value of the current measurements over the second half of a window divided by half the time window duration. The maximum window duration is 10 ms and should consist of a minimum of forty current measurement samples. The time interval between the starts of successive time windows shall not exceed 20% of the time window duration.

Load maximum current ripple: The maximum root mean square magnitude of the steady state non-DC component of the current waveform of a load.

Load maximum inrush current: The peak instantaneous current which flows upon energizing the load or part thereof.

Load maximum pulse load (control negotiations): The maximum change in current allowable for a load that can be negotiated between the load and the electric plant control system. The change is calculated using the same method as for the Load maximum pulse load (no control negotiations)

Load maximum pulse load (no control negotiations): The maximum change in current allowable for a load if a larger value has not been pre-negotiated between the load and the electric plant control system. The change is calculated as the difference between the minimum and maximum load current over a moving time window of 1 second in duration. The time interval between the starts of time windows for calculating the difference shall not exceed 50 ms. The 1s time window is divided into 200 equal sub-windows of 5 ms each. The average load is calculated for each sub-window using a minimum of 20 samples. The minimum load is that of the sub-window with the lowest average load and the maximum load is that of the sub-window with the highest average load.

Load maximum steady state voltage ripple: The maximum root mean square value of the non-DC component of the voltage measured at the input of a load.

Load normal service steady state voltage range: The range of steady state DC voltage that when applied to loads (with the source maximum steady state voltage ripple), the loads are required to work properly. This range accounts for potential voltage drop in the distribution system as well as the Source steady-state voltage range.

Load voltage interruption Tolerance time: The duration of power interruption that a load can tolerate without any change in operation and without damage.

Load Voltage transient Recovery Time: The maximum time for the voltage waveform at the load to return to the range specified by the Load steady-state voltage range (0 to rated power) and Load maximum steady state voltage ripple.

Load Voltage transient Tolerance: Maximum permitted departure from the final steady-state voltage during transient conditions for which the load must remain fully operational.

Mission Critical Equipment: Equipment that is part of mission critical systems and required to operate through emergency conditions. See T9300-AF-PRO-020.

Nominal System Voltage: The design system DC voltage. Used as a reference for establishing other power quality requirements.

Source maximum current ripple: The ripple current a source can provide while still meeting voltage power quality requirements

Source maximum steady state current limit: The maximum steady-state current a source will provide.

Source maximum steady state current ripple: The maximum root mean square value of the non-DC component of the current measured at the output of an online source for which a source must be able to maintain voltage power quality.

Source maximum steady state voltage ripple: The maximum root mean square value of the non-DC component of the voltage measured at the output of an online source.

Source steady-state voltage range (0 to rated power): The allowable variation in the system DC voltage measured at the output of an online source under normal droop operation and constant power mode. This range does not account for potential voltage loss in the distribution system.

Source steady-state voltage range (constant current): The allowable variation in the system DC voltage measured at the output of an online source under current limit operation. This range does not account for potential voltage loss in the distribution system. The current is limited to the rated power divided by the upper limit of the source steady-state voltage range.

Source steady-state voltage tolerance: The maximum deviation of the steady-state voltage measured at the output of an online source from the commanded reference voltage.

Source Voltage transient Recovery Time: The maximum time for the voltage waveform at the source to return to the range specified by the Source steady-state voltage range (0 to rated power) and Source maximum steady state voltage ripple. The Voltage transient recovery time is characterized by the time constants associated with voltage regulation of the sources.

Source Voltage transient Tolerance: Maximum permitted departure from the final steady-state voltage during transient conditions for a single source with the sudden application of load, and with the sudden removal of load.

Temperature Stability: Temperature stability is achieved when the variation between successive temperature measurements at the same location does not exceed 1° C after 30 minutes.

Voltage Spike Waveform: A description of the shape and magnitude of a voltage spike

Worst Case voltage offset from Negative Terminal to Ground: In the case that the Positive Terminal experiences a ground-fault, or in the case of a ground fault in a power source, the maximum magnitude steady-state (negative) DC voltage with respect to ground expected on the Negative Terminal.

Worst Case voltage offset from Positive Terminal to Ground: In the case that the Negative Terminal experiences a ground-fault, or in the case of a ground fault in a power source, the maximum magnitude steady-state DC voltage with respect to ground expected on the Positive Terminal.