Model Description Document
Notional Four Zone MVDC Shipboard Power System Model

Document developed by
ESRDC Team

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Version 3.0

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MISSION STATEMENT

The Electric Ship Research and Development Consortium brings together in a single entity the combined programs and resources of leading electric power research institutions to advance near- to mid-term electric ship concepts. The consortium is supported through a grant from the United States Office of Naval Research.

REVISION HISTORY

VERSION NUMBER	DATE	COMMENTS
1.0	10/20/17	Initial Version of the document
2.0	01/02/19	Sanitized version of document prepared for approval from ONR
2.1	02/06/19	Revised version of 2.0 – Edited document for clearance based on comments
3.0	10/05/20	Revision of the document with description of PCM1A downstream and control system description. Added example implementation and data for converter models

Table of Contents

List of Figures

List of Tables

Terminology and Acronyms

MVDC	Medium Voltage DC
SPS	Shipboard Power System
MBW	Medium Bandwith
DRTS	Digital Real Time Simulator
RTDS^{TM}	Real Time Digital Simulator from RTDS Technologies, Inc.
CHIL	Controller Hardware-in-the-loop
PHIL	Power Hardware-in-the-loop
ESRDC	Electric Ship Research and Development Consortium
DC	Direct Current
AC	Alternating Current
DRTS	Digital Real Time Simulator
CHIL	Controller Hardware-in-the-Loop
PGM	Power Generation Module
PCM	Power Conversion Module
PMM	Propulsion Motor Module
PCC	Point of Common Coupling
MMC	Modular Multi-level Converter
TCR	Thyristor Controlled Rectifier
RoS	Rest of System
NA	Not Applicable

Revision Summary

Major changes to the document revision are described in this section.

Version 3.0

Versio

1 Introduction

The following document provides information regarding documentation of the 'Notional Four Zone MVDC Shipboard Power System Model'. The notional model is based on the IEEE-1826 zonal architecture utilizing MVDC breakerless shipboard power system (SPS) and as presented in [1][2][3][4]. Under previous grant funding through the ESRDC, a notional two zone 12 kV MVDC SPS model was implemented in DRTS platform, RSCAD/RTDS which was primarily intended for use in system fault management studies [5].

To broaden the scope of study and provide a common platform for ESRDC team members for input, discussion and collaboration between various entities in order to achieve the goals laid out by ESRDC, a simulation model working group titled, 'ESRDC Time Domain Electric Model Simulation Working Group' was realized. The goal of the group is to arrive at a common SPS model with its characteristics defined such that implementation of the SPS model in various simulation platforms can be mapped, verified and validated. The model zonal structure provided here is a direct mapping of the 10k ton ship model available in S3D under the ESRDC initiative [6]. The base architectural system data provided here is also derived from the S3D platform. Any dynamic data that is not available through S3D has been derived through discussion at the ESRDC Time-Domain Electrical Simulation Model Working Group. Only electrical characteristics have been considered in this document. Implementation of the power system model on various simulation platforms will be included as a subsidiary document.

Section 2 of this document lists the purpose of the document and the model. Section 3 provides an overview of the zonal architecture as envisioned by the Navy and the ESRDC team. Section 4 highlights the various modules and components that make up the next generation naval warship. While previous sections focus on the architecture of the system model and its components, sections 5 and 6 provides information regarding the data required for implementation of modules, their inherent functionality, performance metrics, and also lays out information regarding electrical coupling of modules, their interface features such as control signal exchange and monitoring to an external control system that is tasked to perform a specific function to SPS such as power management, energy management, fault management and so on.

The data and information provided in this documentation will be used for implementation of the SPS model in various simulation platforms such as RSCAD/RTDS, OPAL-RT, Matlab-Simulink.

2 Purpose

- The model described herein is intended for Medium Bandwidth (MBW) simulation of system where in the time-step, Δt is bound within limits: ($25\ \mu s \leq \Delta t \geq 50\ \mu s$)
- The notional four zone MVDC SPS model described in this document is intended to be platform agnostic and can be implemented on various simulation platforms with the intent to run in real time on various DRTS platforms such as RSCAD/RTDS, OPAL-RT, Typhoon-HIL, etc.
- The suggested characteristics/requirements of the system model described herein should be incorporated into various simulation platforms
- The model described in this document will support controls evaluation. More specifically, the model design will allow efficiently interfacing a diverse set of controls through a well-defined interface in a modular manner. Such controls may be in various forms including software only or a given hardware controller with embedded control logic. Controls can be evaluated by modifying model parameters and observing system responses.
- The characterized system model presented here in will aid in various efforts under the ESRDC project aiming to study areas such as control architecture, advanced control algorithms and strategies, stability

analysis, fault management, energy storage, power and energy management, electric plant load analysis and more

- The information, data and characteristics provided in this document should help with traceability, verification and validation of the SPS model implementation across various simulation platforms since their implementation may vary between different simulation platforms and also on type of model implementation

3 Four zone shipboard power system architecture

Figure 1 shows the proposed notional four zone system architecture. The architecture is derived directly from the 10k ton ship study in S3D and can be mapped directly to it [6]. MVDC at 12 kV will be the primary means of power distribution with a SPS power rating of 100 MW. Each zone will consist of modules such as power generation module (PGM), power conversion module (PCM-1A), integrated power node center (IPNC), propulsion motor module (PMM), energy storage module (ESM). Special loads designated as high ramp rate loads (HRRL) have also been incorporated into the model. Table 1 lists the salient features of the proposed shipboard power system model.

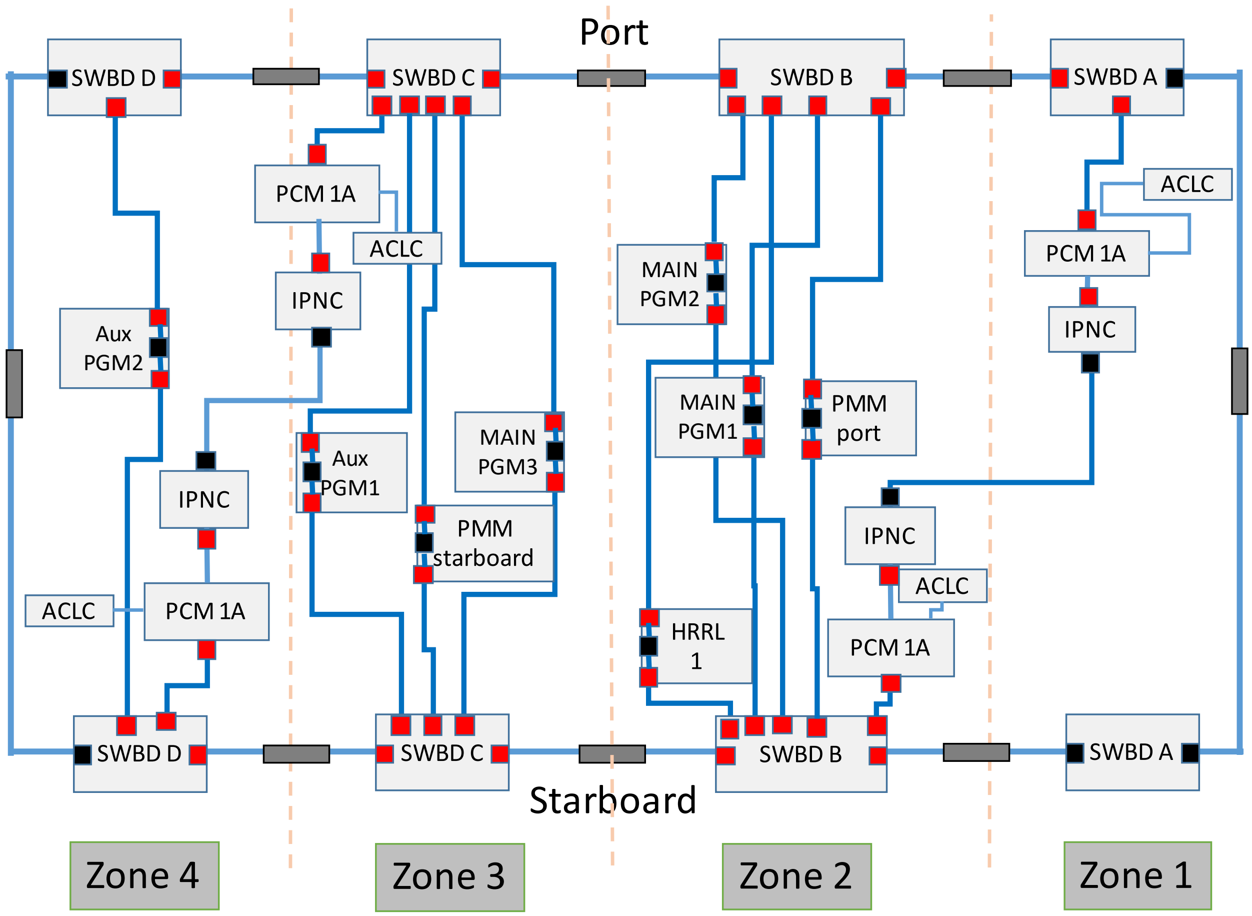

Figure 1 Notional four zone MVDC SPS architecture

Table 1 12 kV, 100 MW shipboard power system model overview

Distribution voltage class		12 kV
Shipboard power generation		~100 MW
Propulsion		72 MW
Special Loads		29.4 MW
Zonal Loads	Hotel	6.31 MW
	Cooling	6.3 MW
Energy Storage		TBD

Salient features and advantages of the zonal architecture of the SPS are described below:

- Zonal architecture of SPS that can support increased reliability and serviceability of loads
- Dual output feed PGMs that when configured appropriately can power port and starboard bus simultaneously and independently
- PGMs with generators running at frequency higher than 60 Hz (120/240 Hz) and the ability to limit fault current through use of power electronic converters
- Energy storage modules that can support un-interruptible loads and aid in special load applications
- Cross zone interconnection of PCM-1A/IPNC for increased serviceability of vital loads through 1kV DC
- The SPS implementation should adhere to the DC voltage interface standards as provided and listed in [7]
- DC disconnect switches implemented throughout the SPS to allow for various system configurations

Table 2 provides breakdown of modules by zones in the SPS model. The SPS model will consist of 3 main PGMs (rated to 30 MW each) and 2 auxiliary PGM (rated to 4 MW each). One PCM-1A will be modeled in each zone. Mission loads will be modeled separately from the aggregated zonal loads. Zonal loads will be further classified into Hotel loads and cooling loads. Hotel loads are further categorized as vital and non-vital hotel loads.

Table 2 SPS model summary by zone

	Zone 1	**Zone 2**	**Zone 3**	**Zone 4**
PGM	One	Two (2- MPGM)	Two (1- MPGM, 1-APGM)	One (1-APGM)
PCM-1A	One	One	One	One
PMM	-	One	One	-
ESM	Two (PCM-1A, IPNC)	Two (PCM-1A, IPNC)	Two (PCM-1A, IPNC)	Two (PCM-1A, IPNC)
Mission Loads (MW)	ML1	HRRL 1 (17) ML2 ML3	ML4 ML5	ML6
Total Hotel Load (MW)	1.47	1.65	1.65	1.54
Cooling Load (MW)	1.26	2.52	1.26	1.26

The sections below provide information on SPS modeling specifically on modeling of modules. Functional, performance, interface, and states of operation for each module represented in the SPS is described below.

4 Components and Modules in SPS

While section 3 provides information regarding the architecture in the SPS, the modules that are be implemented in the SPS model are described below. Information regarding their requirements have been described in section 0.

4.1 MVDC Distribution System

The MVDC distribution voltage will be 12 kV. The MVDC distribution system supports the option of running in either isolated bus mode (port and starboard bus isolated), or parallel mode through various configurations that can be achieved by MV disconnect switch combinations. Table 13 provides information regarding cable sections and their proposed lengths using data provided in 7.1. Although cable lengths are provided, the impedance of the cable in most cases are too small to be properly represented in MBW simulations and can be neglected.

4.2 Power Generation Module

The power generation module (PGM), is the primary power generating unit on the ship. The PGMs can be broadly classified into two types: main PGM (MPGM) and auxiliary PGM (APGM). The main PGMs have a larger generation capacity while the auxiliary PGM will have a fractional generation capacity of MPGM (<30%). Regardless of main or auxiliary PGM, they will comprise of following components: generator, gas turbine, exciter, voltage regulator, rectifier as well as filtering modules based on rectifier topology. Figure 2 shows the block diagram of PGM. The PGM consists of a 120 Hz dual wound single shaft gas turbine generator with two independent sets of 3 phase windings with a gas turbine governor and an excitation system with voltage regulator. The rectifier topology is not fixed and can be any topology as long as it adheres to DC voltage interface standards. The example option for rectifier topology given in this document is for a thyristor controlled rectifier (TCR). Two six pulse TCR each rated to half rating of PGM each fed by one set of the 3-phase windings will convert AC power to 12 kV DC. In some instances, a filter module may be present on the output of the rectifier. Based on the disconnect switch configuration, the two PGM output rectifiers can power either port or starboard independently or power the same bus. Table 3 lists ratings of each PGM in the zonal SPS along with its rectifier ratings in case of a TCR based PGM.

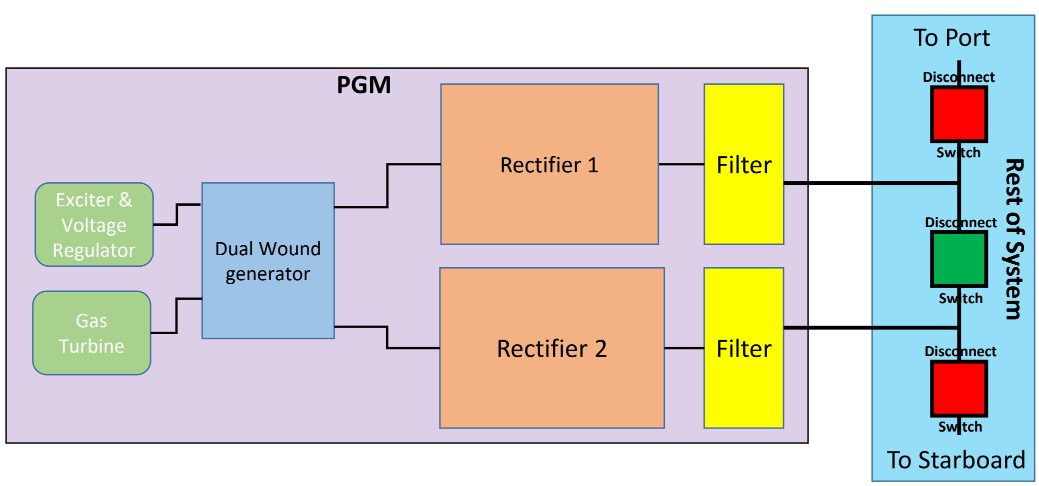

Figure 2 Block diagram of PGM

Table 3 PGM rectifier and generator ratings based on TCR based PGM

	Zone	Generator Nominal Power Rating (MW)	Total Rectifier Power Rating (MW)
Main PGM 1	2	29	34.8
Main PGM 2	2	29	34.8
Main PGM 3	3	29	34.8
Aux PGM 1	3	4.7	5
Aux PGM 2	3	4.7	5

4.3 Power Conversion Module – 1 A

The power conversion module (PCM1A) consists of converter/s that distribute the 12 kV MVDC power to loads at appropriate voltage levels (1 kV DC, 450 V AC). The PCM-1A can be rated up to 11 MW. The PCM1A hosts all the low voltage loads. Figure 3 shows the block diagram of PCM-1A all the downstream components. There exists redundant feeds from neighboring zone at several load center points, which are normally open. Table 4 provides the ratings of the four PCM-1A 12-1 kV dc-dc converter in the SPS model. At the 1 kV bus of PCM1A, several components are interfaced.

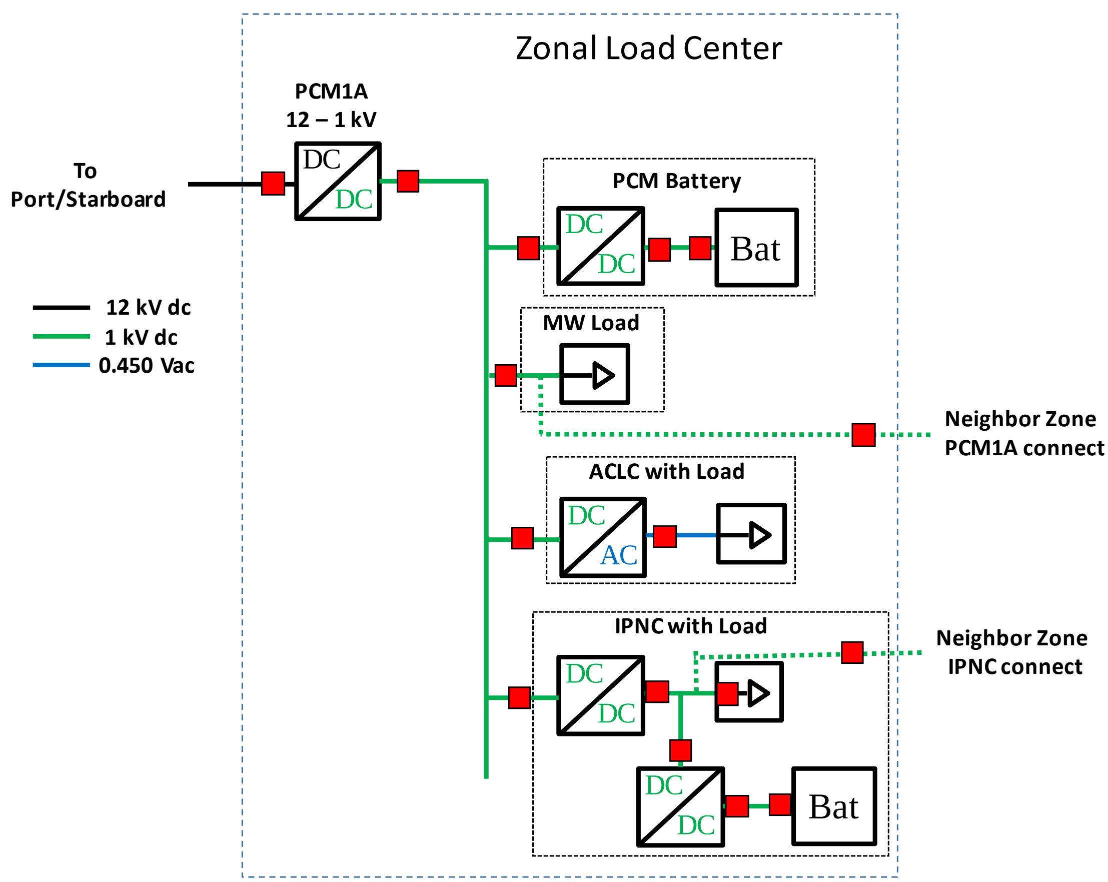

Figure 3 PCM1A with downstream system

Table 4 PCM-1A ratings in SPS model

	Location	**Power rating (MW)**
PCM-1A - 1	Zone 1	10.64
PCM-1A - 2	Zone 2	10.64
PCM-1A - 3	Zone 3	9.17
PCM-1A - 4	Zone 4	9.17

4.3.1 PCM1A battery system

A Lithium-ion battery system is interfaced the 1 kV dc bus through an interface converter. The PCM1A battery system can be utilized by a system level controller to aid in load shaping, relieving generator overloading or any other functionality that the battery system can support. The size of the battery system can be decided based on desired functionality.

4.3.2 MW load

Certain mission and service loads are modeled directly at 1 kV. These loads are lumped under the class MW load. A redundant feed from neighboring zone is available which is open under normal operation.

Table 5 MW Load power rating by zones

Zone	**Power rating (MW)**
1	2
2	2
3	1.5
4	1.5

4.3.3 Integrated Power Node Center

The IPNC hosts mainly mission loads which are also of type uninterruptible. Since the loads served under IPNC require high power quality, another dedicated 1 – 1 kV dc-dc converter is utilized. An IPNC battery system is also implemented which primarily serves the UPS functionality. Table 6 provides ratings of IPNC dc-dc converter by zone. IPNC loads also has a redundant feed from neighbor zone IPNC which is normally open.

Table 6 IPNC power rating by zones

Zone	**Power rating (MW)**
1	2.77
2	3.13
3	3.95
4	1.99

4.3.4 AC Load Center

The AC load center (ACLC) hosts all the 450 V ac loads. ACLC consists of an inverter that powers 450 V loads. The 450 V loads can be classified into two types, service loads and cooling loads. Each zone in the system has 8 loads modeled. Table 7 provides ratings of all loads modeled under ACLC.

Table 7 ACLC Load ratings

Equipment Name	Cruise Electrical Load (kW)	Mission Electrical Load (kW)	Cruise Cooling Load (kW)	Mission Cooling Load (kW)
Vital Loads				
Zone 1	622	788	248.8	315.2
Zone 2	761	1013	304.4	405.2
Zone 3	761	1013	304.4	405.2
Zone 4	751	916	300.4	366.4
Non-vital Loads				
Zone 1	293	163	117.2	65.2
Zone 2	371	191	148.4	86.4
Zone 3	378	199	151.2	79.6
Zone 4	382	163	152.8	65.2

As mentioned in the section 1, the document described here in only focuses on electrical system plant simulation. If a thermal-fluid (TF) system simulation is to be conducted, the TF system will be modeled on a different simulation platform which could run in tandem with DRTS model as co-simulation of electrical and thermal system. In the event that the TF system is present, in that case, appropriate loads could be interfaced and modified as pertaining to the TF system.

4.4 Propulsion Motor Module

Two PMMs, one in zone 2 and zone3 with each rated to 36 MW will be implemented in the model. PMMs will be powered through both port and starboard busses simultaneously. PMMs will be implemented such that balanced power drawn from both busses. Figure 4 shows the block diagram of PMM. If detailed implementation off PMM is not required, for a simplified version of PMM, see section 7.6 for an implementation example.

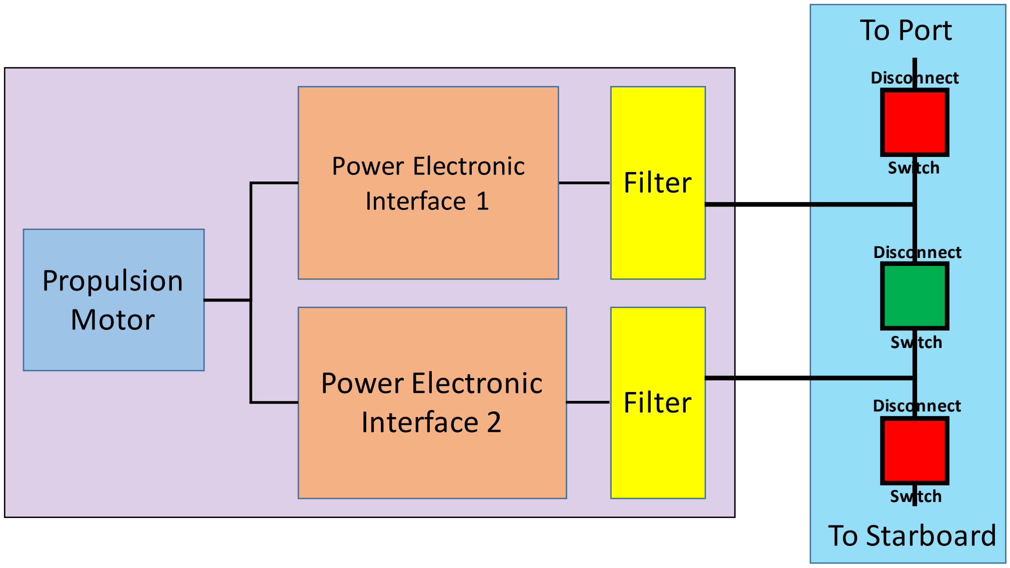

Figure 4 Block diagram of PMM

4.5 High Ramp Rate load

The HRRL load is large load powered through MVDC bus. This load is rated to 20 MW. Due to the nature of the load, the load is interfaced through power converters and energy storage elements such that large ramps and pulses of the load are not observed on the MVDC bus. The energy storage for the HRRL could be a hybrid storage system which incorporates power dense as well as energy dense storage elements. An example implementation of HRRL load is provided in section 7.7

5 Requirements and Characteristics

The system requirements provided in this section aims to describe desired characteristics from each module w.r.t implementation and operation. The requirements are classified into

- Functional: Intended purpose of the module/component and its scope of study
- Performance: capability of the module/component
- Interface: physical and control interfaces required to accomplish the purpose of the module/component. The interface characteristics provide a digital link to the control system to exchange data and information between the module and control system to enable the control of module. While certain desired power system characteristics can be controlled through the use of interface signals, certain characteristics are inherent to module implementation and can be set using the configurable parameters of the model
- States/mode: default and fault behavior of module/component. There can be multiple normal modes of operation for a specific module out of which one such mode should be selected as default

5.1 DC disconnect Switch

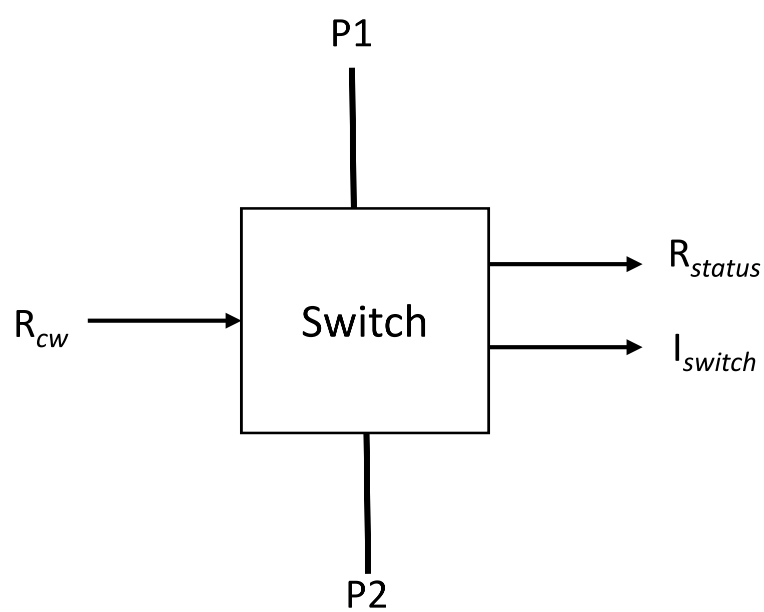

Figure 5 DC disconnect switch signal diagram

DC disconnect switches will be assumed as the primary type of interruption devices for 12 kV and 1 kV DC unless specified as a DC breaker. Figure 5 shows the signal block diagram of a DC disconnect switch depicting various signals in and out of the component. Figure 5 provides information regarding the interface and monitoring signals from disconnect switch.

Table 8 Disconnect switch interface and control signal descriptions

Name	Description	Default	Unit

P1	Switch Primary Electrical Interface	-	kV
P2	Switch Secondary Electrical Interface	-	kV
R_{cw}	Switch isolation control word	-	-
R_{status}	Switch status	-	-
I_{switch}	Current through secondary of switch	-	kA

5.1.1 Functional requirements

The DC disconnect switch is intended to provide isolation between various modules in the system for normal operation and for the ability to provide system reconfiguration. The switches in the system are not intended to be used for studies related to degradation of switch performance and internal breakdown/malfunction of switches.

5.1.2 Performance characteristics

NA

5.1.3 Interface signals

Table 8 provides a list of signals for interface and control signals.

5.1.4 States and Modes of Operation

- The disconnect switch can only be in one of two states, either CLOSED or OPEN
- The default mode can be either one of the states based on desired system configuration
- Disconnect switch open operation is blocked if current through the switch is higher than 20 A and/or v potential difference across the two sides of the switch is greater than 50 V
- Disconnect switch close operation is blocked if potential difference across the switch is higher than 50 V

5.2 Power Generation Module

Figure 6 shows the signal block diagram of a power generation module depicting various signals in and out of the component. PGM module shown above consists of a dual wound generator with two rectifiers (with incorporated filtering system), and AC breakers. Figure 6 provides information regarding the signal type, their functions, range and description of the signal.

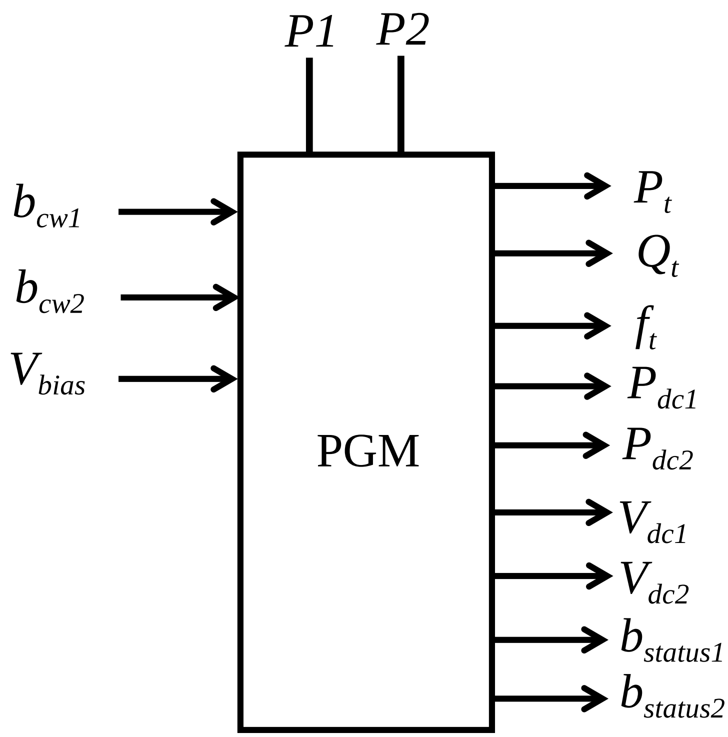

Figure 6 PGM interface signal diagram

5.2.1 PGM Functional requirements

The following functional requirements are applicable to all main and auxiliary PGMs:

- The PGM is required to provide power to the MVDC distribution at 12 kV while maintaining DC voltage interface standards
- The generators are required to be within operational limits for frequency and voltage
- Support load sharing between PGM rectifiers
- Provide self-protection capability in case of malfunction of fault management system
- Although real time simulations are not advisable for long term SPS fuel efficiency cost studies, provisions in the model should be available to accommodate such studies

5.2.2 PGM Performance characteristics

The desired performance characteristics for PGMs are described below.

- Generator real power ramp rate should be controllable by the user and can be set specific to a certain study
- Generator efficiency curve should be made accessible if necessary
- Provisions to set rectifier maximum power ramp rate

- Able to control current limiting capability of rectifiers
- Control (block) of firing pulses of rectifiers where modeled using switching converters
- The PGM module should be able to assist load sharing control with proper inputs and be able to accept the load share command request (voltage/current bias) based on the mode of operation. For any PGMs operating in voltage source mode (VSM), a voltage bias signal will be required and for any PGM operating in current source mode (CSM), a current bias signal is to be provided. In most case studies, the PGMs will be operated in VSM mode as opposed to CSM

Table 9 PGM interface and control signal descriptions

Name	Description	Default	Unit
P1	Rectifier 1 three phase power interface to MVDC bus	-	-
P2	Rectifier 2 three phase power interface to MVDC bus	-	-
b_{cw1}	PGM generator three phase winding 1 AC breaker	-	-
b_{cw2}	PGM generator three phase winding 2 AC breaker	-	-
V_{bias}	Voltage bias to PGM control system from system level load sharing control. See section 7.2.1.4 for details on output voltage control of PGM		
Pt	AC generator real power output	-	MW
Qt	AC generator reactive power output	-	Mvar
ft	AC generator frequency	-	Hz
P_{dc1}	PGM measured output real power from terminal P1	-	MW
V_{dc1}	PGM output dc voltage from terminal P1	-	kV
P_{dc2}	PGM measured output real power from terminal P1	-	MW
V_{dc2}	PGM output dc voltage fro00m terminal P1	-	kV
$b_{status1}$	AC breaker status for three phase set winding 1	-	-
$b_{status2}$	AC breaker status for three phase set winding 2	-	-

5.2.3 PGM Interface signals

Table 9 provides a list of signals for interface requirements pertaining to control and monitoring signals.

5.2.4 PGM States and Modes of Operation

- Under normal mode of operation, PGMs should be able to provide dual output for interfacing to MVDC system
- In the event of a fault on the 12 kV DC side, the PGM rectifiers should act accordingly and be able to block firing pulses if requested by the fault management system.
- In the event of a fault on the AC bus between generator and rectifiers, the PGM should power down and disconnect from RoS.
- Fault management in the system should be able to detect fault on the MVDC system in less than 2 ms. In case of undetected fault in the system or miss-operation of fault management system, PGM should go into self-protection mode and if observed current limitation is observed by PGM for more than 3 ms, it should ramp down voltage and current and disconnect from RoS unless specified by fault management system

5.3 Power Conversion Module

Since PCM1A is comprised of several modules that have been discussed in sections 7.3, interface descriptions have not been laid out.

5.3.1 PCM-1A Functional requirements

The following functional requirements are applicable to PCM-1A:

- PCM-1A is required to service all loads connected through it while maintain AC and DC voltage interface standards
- Provide self-protection capability in case of malfunction of fault management system
- Optional energy storage module if present in the system should be set such that default mode of operation is to improve system stability by reflecting the PCM-1A load on 12 kV DC side observable as constant impedance type
- Support system level power and energy management by providing appropriate interfaces

5.3.2 PCM-1A Performance characteristics

- PCM-1A should be able to provide current limiting functionality for each converters modeled in the module
- Converters within PCM-1A should be able to support adjustable power ramp rate
- Efficiency modeling of converters should be supported
- Disconnect switches and breakers within PCM-1A should be able to support the fault management system. In case of non/miss-operation of FMS, self-protection of PCM-1A should be required

5.3.3 PCM-1A Interface signals

5.3.4 PCM-1A States and Modes of Operation

- Under normal mode of operation of PCM-1A, all loads will be served as requested by PCM-1A
- Self-protection modes of PCM-1A is described below:
    - For a fault on 1 kV DC bus of PCM-1A, all disconnect switches within PCM-1A open
    - For a fault on 450 V AC bus of ACLC, appropriate switches open to isolate fault
    - For a fault on 1 kV DC bus supplying MW class load, appropriate switches open to isolate fault
    - For a fault on 1 kV DC bus supplying IPNC, appropriate switches open to isolate fault

5.4 Energy Storage Module

Figure 7 shows the signal block diagram of an energy storage module. The energy storage module can be either directly connected to the desired bus or interfaced through a converter based on system requirements.

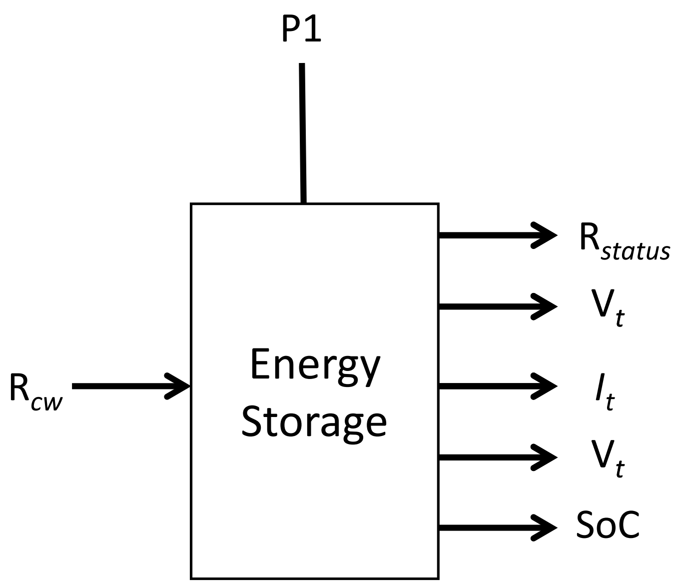

Figure 7 ESM signal diagram

5.4.1 ESM Functional requirements

The following functional requirements are applicable to ESM:

- ESM is required to support SPS in case of power interruption, serves mission loads that require pulsed power characteristics
- Although charge/discharge cycle count can be monitored, degradation studies of ESM are not applicable to this model

Table 10 ESM interface and control signal descriptions

Name	Description	Default	Unit
P1	Energy storage element power interface to LVDC bus	-	-
R_{cw}	Energy storage isolation device control word	-	-
R_{status}	Energy storage isolation device status	-	-
V_t	Energy storage terminal voltage	-	kV
I_i	Energy storage terminal current	-	kA
SoC	Energy storage State of Charge	-	pu

5.4.2 ESM Performance characteristics

- ESM should be able to provide State of Charge (SoC) information at all times

5.4.3 ESM Interface signals

Table 10 provides a list of signals for interface requirements pertaining to control and monitoring signals.

5.4.4 ESM States ad Modes of Operation

- ESM should be either be in standby mode or in operation based on the intended use
- During a fault on the internal ESM bus, the appropriate disconnect switch should operate to isolate the fault

5.5 Propulsion Motor Module (TBD)

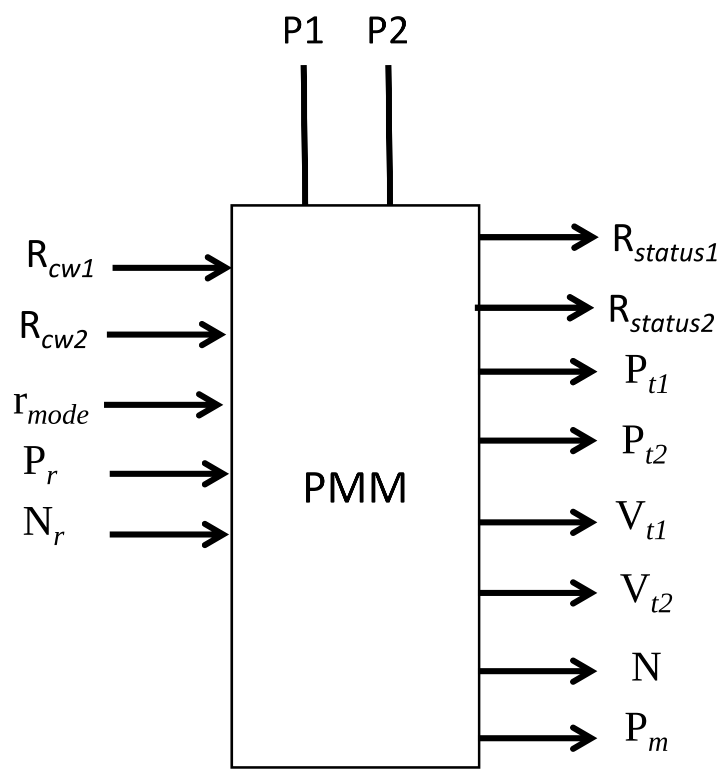

Figure 8 PMM interface signal

5.5.1 PMM functional requirements

- PMM module should be switch between modes of operations
- PMM should maintain speed/power as requested by user

5.5.2 PMM performance characteristics

- When in speed mode, the PMM should maintain the requested speed
- When in power mode, PMM should draw appropriate power as requested

5.5.3 PMM interface signals

Table 11 provides PMM interface signal description.

Table 11 PMM interface and control signal descriptions

Name	Description	Default	Unit
P1	Input 1 interface to MVDC bus	-	-
P2	Input 2 interface to MVDC bus	-	-
r_{cw1}	Input 1 isolation device control word	-	-
r_{cw2}	Input 1 isolation device control word	-	-
r_{mode}	PMM mode select: speed/power		-
P*r*	Power request to PMM	-	MW
N*r*	Speed request to PMM	-	knot
P*t1*	Input 1 measured power	-	MW
P*t2*	Input 1 measured power	-	MW
V*t1*	Input 1 measured dc voltage	-	kV
V*t2*	Input 1 measured dc voltage	-	kV
P*m*	PMM motor measured real power	-	MW
N	Measured speed	-	knot
$r_{status1}$	Input 1 isolation device status	-	-
$r_{status2}$	Input 2 isolation device status	-	-

5.6 HRRL (TBD)

5.6.1 HRRL functional requirements

- PMM module should be switch between modes of operations
- PMM should maintain speed/power as requested by user

5.6.2 HRRL performance characteristics

- When in speed mode, the PMM should maintain the requested speed
- When in power mode, PMM should draw appropriate power as requested

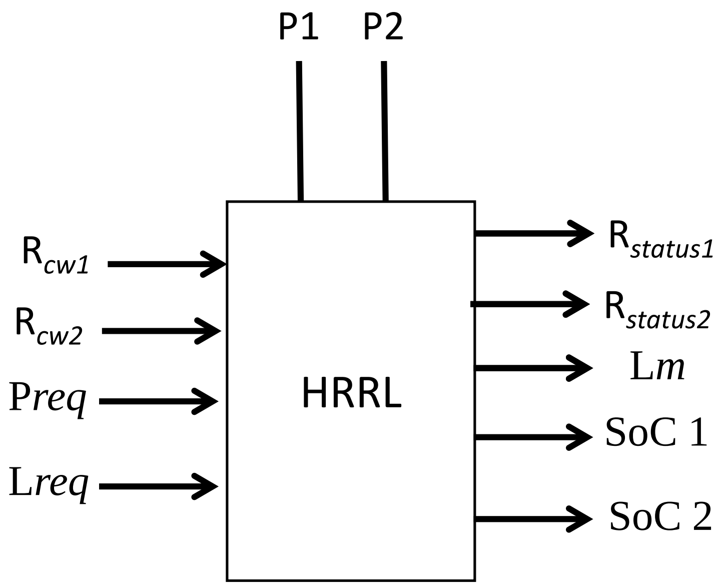

Figure 9 HRRL interface and control signal diagram

5.6.3 HRRL interface signals

Table 12 provides PMM interface signal description.

Table 12 HRRL interface and control signal descriptions

Name	Description	Default	Unit
P1	Input 1 interface to MVDC bus	-	-
P2	Input 2 interface to MVDC bus	-	-
r_{cw1}	Input 1 isolation device control word	-	-
r_{cw2}	Input 1 isolation device control word	-	-
P*req*	Power request to charge energy storage 'Esa' (high energy storage system)	-	MW
L*req*	HRRL load demand	-	MW
L*m*	Measured HRRL load	-	MW
SoC 1	State of Charge of high energy storage element	-	pu
SoC 2	State of Charge of high power storage element	-	pu
V*t1*	Input 1 measured dc voltage	-	kV
V*t2*	Input 1 measured dc voltage	-	kV
P*m*	PMM motor measured real power	-	MW
N	Measured speed	-	knot
$r_{status1}$	Input 1 isolation device status	-	-
$r_{status2}$	Input 2 isolation device status	-	-

6 Baseline System Level Controls

This section provides information regarding baseline system level controls that should be present for the model

6.1 PGM load sharing controls

A load sharing scheme between PGMs should be available so that any online PGMs should share the load proportional to their configuration.

6.2 Load shedding scheme

The load shedding scheme should provide granularity in dropping loads, i.e., considers port- and starboard connections separately. This revised approach allows simulating a refined overload handling. The new scheme is based on a stage based load shedding as depicted in Figure 10. Based on the monitored generator loading, timed load shedding is performed while considering the load designation, i.e., non-vital, semi-vital, or vital. Furthermore, this scheme is implemented for port- and starboard connected loads, respectively. The settings used reflect the load level in per-unit (i.e., 1 pu) and the pick-up times (i.e., 250 ms, 2.5 s, and 5 s). The load classifications reflect and include non-mission loads (non-vital) to critical mission loads. Load shedding capabilities also include portion of the propulsion by limiting to half of the requested demand. The actual loads that are shed can be interchanged based on mission priority but for the cases herein, one set of selected loads is used.

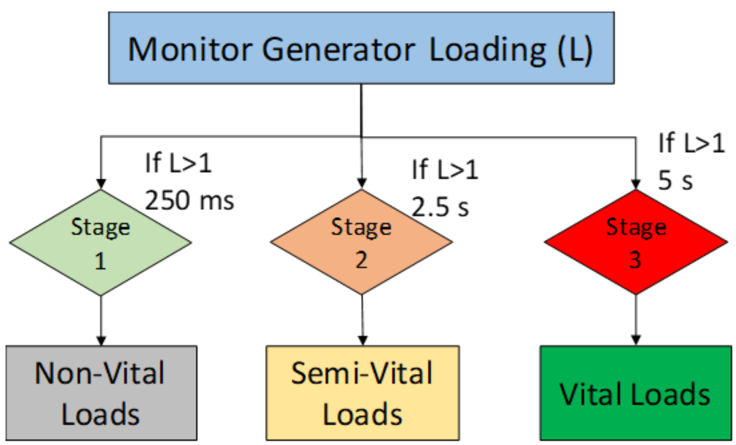

Figure 10 Stage based load shedding scheme

6.3 PGM protection

The PGM self protection scheme should be implemented such that under adverse system condition or mal-operation of PGM, the PGM isolates itself from the rest of the ship.

References

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7 Example Models

7.1 Cable Data

Table 13 SPS model MVDC cable information

Cable No	Description	Length (m)
CS 1	Port side Zone 1 to Zone 2 switchboard	57.13
CS 2	Port side Zone 2 to Zone 3 switchboard	38
CS 3	Port side Zone 3 to Zone 4 switchboard	34.16
CS 4	Port to Starboard cross connection Zone 4	
CS 5	Starboard side Zone 1 to Zone 2 switchboard	15.11
CS 6	Starboard side Zone 2 to Zone 3 switchboard	43.33
CS 7	Starboard side Zone 3 to Zone 4 switchboard	50.65
CS 8	Port to Starboard cross connection Zone 1	
CS 9	EDG to Port Zone 1 connection	19.72
CS 10	EDG to Starboard Zone 1 connection	9.46
CS 11	MPGM 1 to Zone 2 Port connection	3.72
CS 12	MPGM 1 to Starboard Zone 2 connection	42.68
CS 13	MPGM 2 to Zone 2 Port connection	17.65
CS 14	MPGM 2 to Starboard Zone 2 connection	27.21
CS 15	MPGM 3 to Zone 3 Port connection	13.3
CS 16	MPGM 3 to Starboard Zone 3 connection	24.95
CS 17	APGM 1 to Zone 3 Port connection	29.63
CS 18	APGM 1 to Starboard Zone 3 connection	7.54
CS 19	APGM 2 to Zone 4 Port connection	4.89
CS 20	APGM 2 to Starboard Zone 4 connection	2.38
CS 21	Zone 1 PCM-1A to Starboard connection	3.77
CS 22	Zone 2 PCM-1A to Port connection	4.02
CS 23	Zone 3 PCM-1A to Starboard connection	2.57
CS 24	Zone 4 PCM-1A to Port connection	8.01
CS 25	Starboard PMM to Zone 2 Port connection	20.39
CS 26	Starboard PMM to Zone 2 Starboard connection	47.08
CS 27	Port PMM to Zone 3 Port connection	9.28
CS 28	Port PMM to Zone 3 Starboard connection	28.86
CS 29	IPNC to VLS Zone 1	9.19
CS 30	IPNC to ADS Starboard Zone 2	35.89
CS 31	Port Integrated topside to Port Zone 2 connection	19.43
CS 32	Port Integrated topside to Starboard Zone 2 connection	36.37
CS 33	Starboard Integrated topside to Port Zone 2 connection	31.07
CS 34	Starboard Integrated topside to Starboard Zone 2 connection	48.01
CS 35	RADAR to Port Zone 2 connection	21.75
CS 36	RADAR to Starboard Zone 2 connection	27.14
CS 37	EMRG to Port Zone 2 connection	27.04
CS 38	EMRG to Starboard Zone 2 connection	11.75
CS 39	RADAR to Port Zone 3 connection	22.32
CS 40	RADAR to Starboard Zone 3 connection	15.54
CS 41	Zone 4 IPNC to LASER connection	26.59

7.2 PGM

The example implementation of PGM utilizes the dual wound machine model running at 120 Hz along with notional gas turbine and excitation system. The gas turbine system used is IEEE GGOV1 while the excitation system is IEEE AC8B.

7.2.1.1 **Dual wound synchronous generator**

Dual wound machine will be considered as the default option for modeling of PGM generators. Alternate generator implementations can be considered when dual wound machine model is not readily available in DRTS library. Parameters for the model have been provided in Table 14.

Table 14. Parameters for Notional Synchronous Machine

Parameter	Description	Default Value
S_r	Rated apparent power (MVA).	37.5
V_r	Rated voltage (line-line, RMS) (kV).	11
f_r	Rated frequency (Hz).	120
Xa	*Stator Leakage Reactance (p.u)*	*0.08*
Xd	*D-axis Unsaturated Reactance (p.u)*	*1.352*
Xd'	*D-axis Unsaturated Transient Reactance (p.u)*	*0.296*
Xd"	*D-axis Unsaturated Sub-Transient Reactance (p.u)*	*0.148*
Xq	*Q-axis Unsaturated Reactance (p.u)*	*0.836*
Xq"	*Q-axis Unsaturated Sub-Transient Reactance (p.u)*	*0.122*
Ra	Stator resistance (pu).	0.006
Tdo'	*D-Axis Unsaturated Transient Open T Constant (sec)*	*4.141*
Tdo"	*D-Axis Unsaturated Sub-Transient Open T Constant (sec)*	*0.027*
Tqo"	*Q-Axis Unsaturated Sub-Transient Open T Constant (sec)*	*0.184*

7.2.1.2 **Gas turbine governor**

IEEE GGOV1 gas turbine governor module is used as the default gas turbine model for the system. Parameters for the model have been provided in Table 15.

Table 15. Parameters for Notional GGOV1 gas turbine governor

Parameter	Description	Default Value
R	Permanent Droop	0.04
Tpelec	Electric Power transducer time constant	0.1 sec
Maxerr	Mac value of speed error signal	0.05 p.u.
Minerr	*Min Value for speed error signal*	*-0.05* p.u.

Kpgov	*Governor proportional gain*	*20*
Kigov	*Governor integral gain*	*10*
Kdgov	*Governor derivative gain*	*4*
Tdgov	*Governor derivative controller time constant*	*1.0 sec*
Vmax	*Maximum valve position limit*	*1.0*
Vmin	*Minimum valve position limit*	*0.15*
Tact	*Actuator time constant*	*0.5 sec*
Kturb	*Turbine gain*	*1.5*
Wfnl	*No load fuel flow*	*0.2* p.u.
Tb	*Turbine lag time constant*	*0.1*
Tc	*Turbine lead time constant*	*0*
Teng	*Transport lag time constant*	*0 sec*
Tfload	*Load limiter time constant*	*3.0 sec*
Kpload	*Load limiter proportional gain*	*2*
Kiload	*Load limiter integral gain*	*0.67*
Ldref	*Load limiter reference value*	*1.0* p.u.
Dm	*Speed sensitivity co-efficient*	*0.0* p.u.
Ropen	*Maximum valve opening rate*	*0.3 pu/sec*
Rclose	*Minimum valve closing rate*	*-0.3* p.u.*/sec*
Kimw	*Power controller (reset) gain*	*0.0*
Aset	*Acceleration limiter setpoint*	*0.01* p.u.*/sec*
Ka	*Acceleration limiter gain*	*10*
Ta	*Acceleration limiter time constant*	*0.1 sec*
Trate	*Turbine MW base*	*Gen MVA*
Db	*Speed governor deadband*	*0*
Tsa	*Temperature detection lead time constant*	*4.0 sec*
Tsb	*Temperature detection lag time constant*	*5.0 sec*
Rup	*Maximum rate of load limit increase*	*99*
Rdown	*Maximum rate of load limit decrease*	*-99*
Rselect	*Feedback signal for governor droop*	*Electric Power Output*
Flag	*Duel source characteristic*	*Speed dependenet*

7.2.1.3 Excitation system

IEEE AC8B is used as the default excitation system. Parameters for the model have been provided in Table 16.

Table 16. Parameters for Simplified IEEE Type AC8B Exciter

Parameter	Description	Default Value
Tr	Regulator input filter time constant (sec)	0.02
k_{PR}	Regulator proportional gain (p.u.)	20
kir	Regulator integral gain (p.u.)	10
kdr	Regulator derivative gain (p.u.)	4
Tdr	Regulator derivative block time constant (sec)	0.05
Vpidmax	PID maximum limit (p.u.)	6.5
Vpidmin	PID minimum limit (p.u.)	0
k_A	Voltage regulator proportional gain (p.u.)	1
T_A	Voltage regulator time constant (sec).	0.001
V_{RMAX}	Voltage regulator upper limit.	6.5
V_{RMIN}	Voltage regulator lower limit.	0
Kc	*Rectifier loading factor (p.u.)*	*0.55*
Kd	*Exciter regulation factor*	*1.1*
Ke	*Exciter field proportional constant* (p.u.)	*1*
Te	*Exciter field time constant (sec)*	*1*
VFEmax	*Exciter field current limit (>0)* (p.u.)	*6*
VEmin	*Minimum exciter output voltage* (p.u.)	*0*
E1	*Field voltage Value 1* (p.u.)	*6.5*
Se1	*Saturation factor at E1*	*0.3*
E2	*Field voltage Value 2* (p.u.)	*7*
Se2	*Saturation factor at E1*	*3.0*
Cal	*Saturation constant A calculation method*	*Abs(A)*

7.2.1.4 Thyristor controlled rectifier (TCR)

The TCR system used comprised of a six pulse rectifier with a rectifier controller. Figure 11 shows the control system for TCR while Figure 12 shows the control structure for TCR. Table 17 provides the parameters for TCR control system.

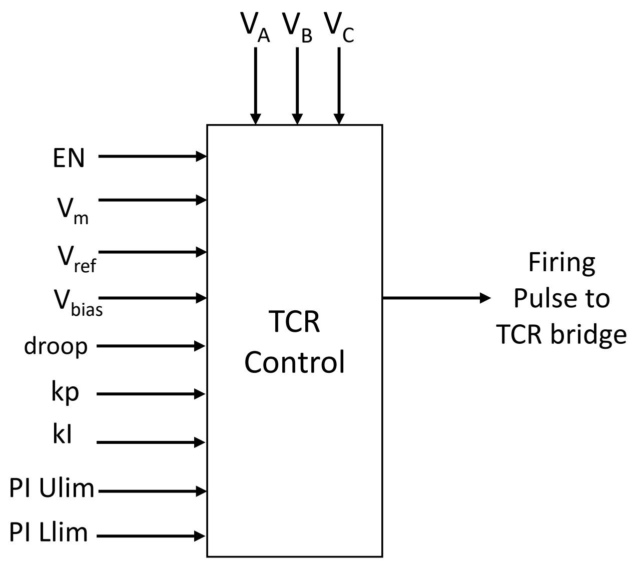

Figure 11 TCR control system

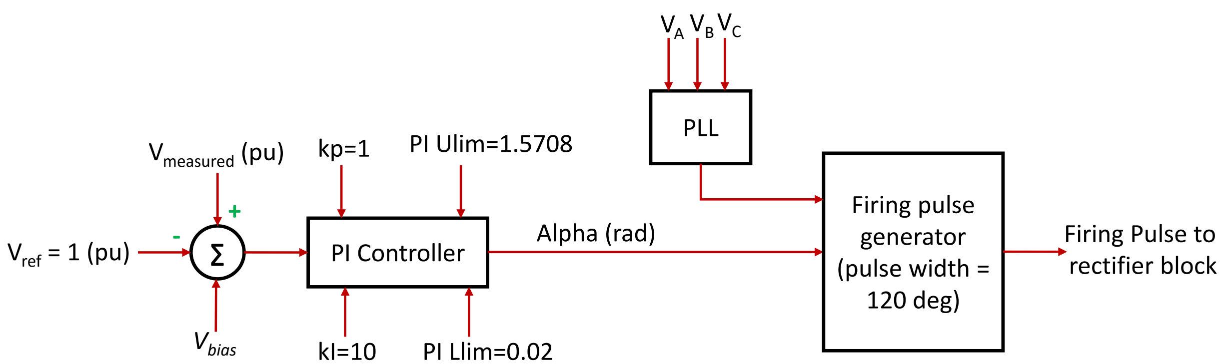

Figure 12 PGM TCR control structure

Table 17 TCR Control parameters

Parameter	Description	Default Value	Unit
EN	TCR control enable	1	NA
Vm	DC measured voltage at PGM terminal	-	kV
Vref	Voltage reference for TCR control	12	kV
Vbias	Voltage bias signal from load sharing system	-	pu
Droop	Droop factor	0.04	-
Kp	PI controller proportional gain	1	-
kI	PI controller integral gain	10	-
PI Ulim	PI regulator output upper limit	1.5708	rad
PI Llim	PI regulator output lower limit	0.002	rad
V_A, V_B, V_C,	Instantaneous AC three phase voltages	-	kV

7.3 DC - DC Converter

The dc-dc converter model described below is used to model several components in the zonal load centers. The converter model is an average value representation rather than explicitly modeling converter control structure, intended to run on DRTS platforms, for medium bandwidth (MBW) simulation studies.

Figure 13 shows the illustration of dc-dc converter implementation on RTDS. Figure 14 shows the dc-dc converter control stage implementation. The model employs a current injection (I_r) on the primary side and a voltage source (V_r) on the secondary side. Input and output quantities to the model are entered in per-unit values. The model is based around the concept of an ideal transformer with adjustable turns ratio, n. The controls accept a reference secondary side voltage, V_2, which is biased through the droop characteristic affected by the difference between the reference power P_2* and the actual output power P_2. This voltage reference is further augmented by the term I_2 Z_2 to compensate for the secondary side voltage drop across Z_2. The voltage reference may be further augmented by the term -I_2 Z_{2e} in order to include voltage drop for an emulated impedance, Z_{2e}. These contributions combine to form the effective voltage reference, V_e. This voltage reference is divided by the primary side voltage, V_1, after applying the filter of $G_{1(s)}$ to this voltage measurement, resulting in the reference turns ratio, n*. Here, $G_{1(s)}$ is intended to represent a restriction in the bandwidth of disturbances on the primary voltage that may propagate through to the secondary side. The filter $G_{2(s)}$, representing the control bandwidth of the converter, is then applied to n*, and the hard limiter is then applied to enforce limits on the minimum and maximum values of the turns ratio. Two other branches are employed to represent the current limiting behavior of the converter. The current limiting functions f1 and f2 provide gains as functions of the primary (I_1) and secondary (I_2) currents, respectively. These gains are typically unity within the current limits of the converter, and these tend to zero as the current limits are approached. Rate limiters 1 and 2 allow these multiplicative factors to ramp down very quickly, but ramp back to unity more slowly in order to avoid rapid oscillations when current limiting. The result of multiplication with these current-limiting factors is the actual turns ratio, n. This factor is multiplied by the filtered primary side voltage to produce the secondary voltage reference, V_r, and it is multiplied by the secondary current to provide the primary side current reference, I_r. Generic parameters for the model along with default values for certain elements have been provided in Table 18.

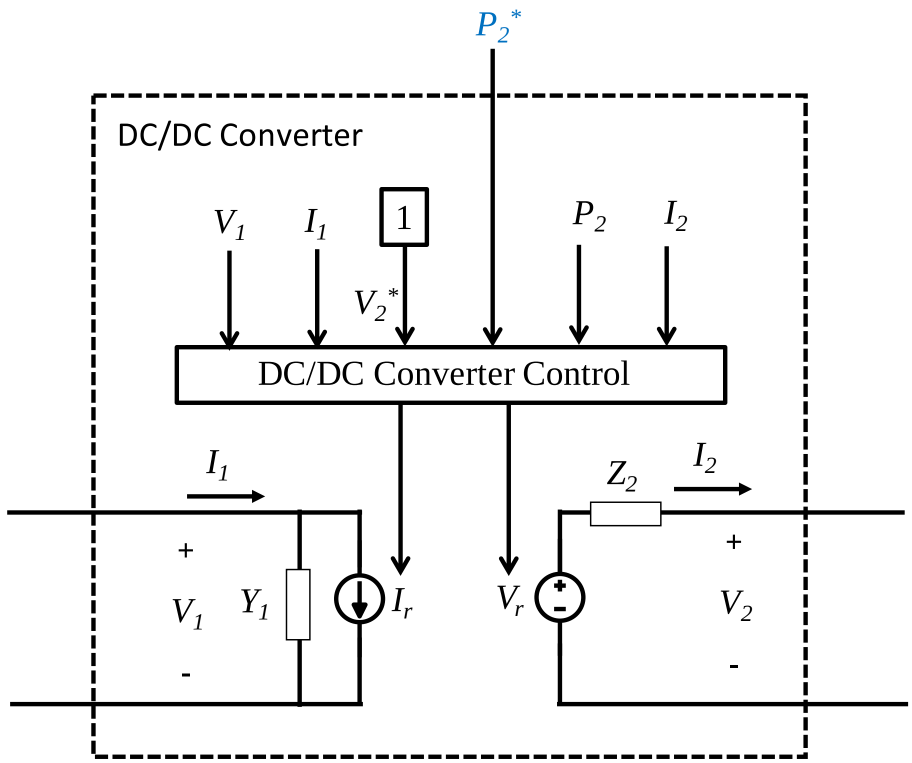

Figure 13 DC-DC Converter Model

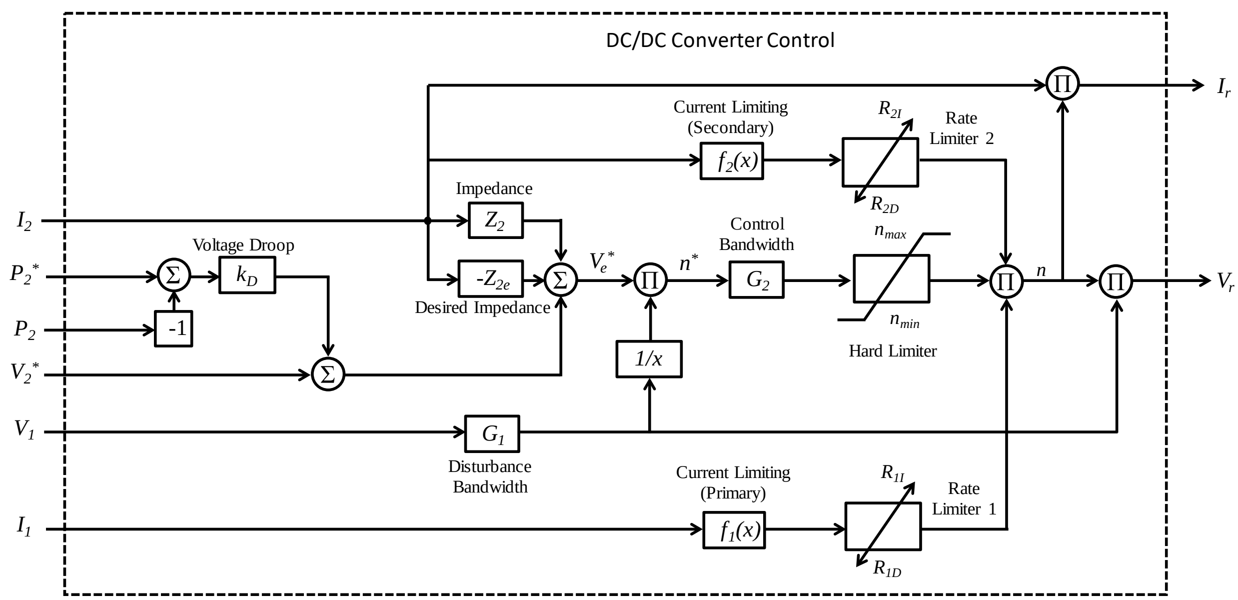

Figure 14 DC-DC converter model control

$$Y1(s) = \frac{1}{R1 - Y1} \qquad \textbf{Eq. 7-1}$$

$$Z2(s) = R1 - Z2 + \frac{s(X1 - Z2)}{2\pi f b} \qquad \textbf{Eq. 7-2}$$

$$Z2e(s) = R1\text{-}Z2e \quad \textbf{Eq. 7-3}$$

$$Gi(s) = \frac{1}{\left(\frac{s}{2\pi fc - Gi}\right) + 1} \quad \textbf{Eq. 7-4}$$

Table 18 Parameters of DC/DC converter

Block	Parameter	Description	Value
N/A	P_{rated}	Converter rated power	Variable (MW)
N/A	$V_{1\text{-}rated}$	Converter primary side voltage	Variable (kV)
N/A	$V_{2\text{-}rated}$	Converter secondary side voltage	Variable (kV)
N/A	f_b	Base frequency for purposes of computing reactive components	60 Hz
N/A	$Z_{b\text{-}1}$	Base impedance on primary side	TBD
N/A	$Z_{b\text{-}2}$	Base impedance on secondary side	TBD
Y1	$R_{1\text{-}Y1}$	Converter input admittance resistive component (see Eq. 7-1)	100 pu
Z2	$R_{1\text{-}z2}$	Converter output impedance resistive component (see Eq. 7-2)	0.01 pu
Z2	$X_{1\text{-}z2}$	Converter output impedance reactance component (see Eq. 7-2)	0.05 pu
Voltage Droop	kD	Voltage droop factor	0.1
Desired Impedance	R_{z2e}	Resistive component of desired impedance (see Eq. 7-3)	0 pu
Disturbance bandwidth	$f_{c\text{-}G1}$	Cutoff frequency for primary-side disturbance (see Eq. 7-4)	800 Hz
Control bandwidth	$f_{c\text{-}G2}$	Cutoff frequency for representing control bandwidth (see Eq. 7-4)	250 Hz
Current limiting (primary)	$f_{1(x)}$	Scale factor function for primary side current limiting (see Table 19 and Figure 15)	N/A
Current limiting (secondary)	$f_{2(x)}$	Scale factor function for secondary side current limiting (see Table 19 and Figure 15)	N/A
Rate limiter 1	R_{I1}	Limit for rate of increase	10 pu/s
Rate limiter 1	R_{D1}	Limit for rate of decrease	-100 pu/s
Rate limiter 2	R_{I2}	Limit for rate of increase	10 pu/s
Rate limiter 2	R_{D2}	Limit for rate of decrease	-100 pu/s

Table 19 DC-DC Converter Scale Factor Function for Current Limiting

Current (pu)	Scale Factor
0	1.0
1.1	1.0
1.25	0.0

1.4	0.0

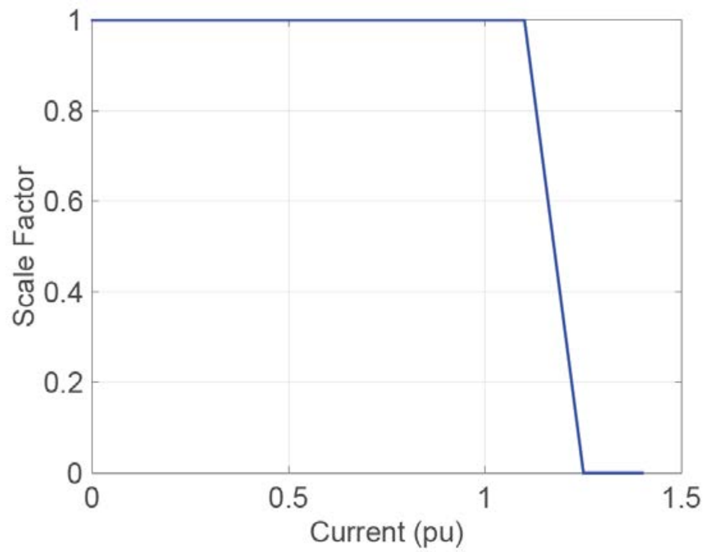

Figure 15 DC-DC Converter Scale Factor Function Current Limiting

7.4 AC-DC Converter

The ac-dc converter model provided here below can be used for rectification of ac to dc power when needed instead of using an elaborate switching level implementation. The converter model is an average value representation rather than explicitly modeling converter control structure, intended to run on DRTS platforms, for medium bandwidth (MBW) simulation studies.

Figure 16 shows the illustration of ac-dc converter implementation on RTDS. Figure 14 shows the dc-dc converter control stage implementation. The model is utilized for a converter controlling the voltage on the secondary side, and, thus, employs a three-phase current injection ($I_{r\text{-}abc}$) on the primary side and a voltage source (V_r) on the secondary side. The controls for the model, illustrated in Figure 17 are based closely on those of the DC/DC converter described in Figure 14. In the case of the AC/DC converter model, a phase-locked loop (PLL) is used to track the voltage angle, Θ. This angle is used to convert the three-phase voltages (V_{1abc}) and currents (I_{1abc}) to DQ-frame quantities V_{1dq} and I_{1dq}, respectively. From these, the magnitudes of the voltage ($|V_1|$) and current ($|I_1|$) are computed, and used in place of the instantaneous primary side voltage and current employed in the DC/DC converter model. Similarly to the DC/DC converter model, the secondary side DC voltage reference, V_r, is computed through the multiplication of the turns ratio, n, with the filtered primary side voltage magnitude, $|V_1|$. The primary side current injections, $I_{r\text{-}abc}$, are computed based on the measured secondary-side power, P_2, and primary-side voltage magnitude, $|V_1|$. These are generated using θ in order to be in phase with the primary side voltages for unity power factor.

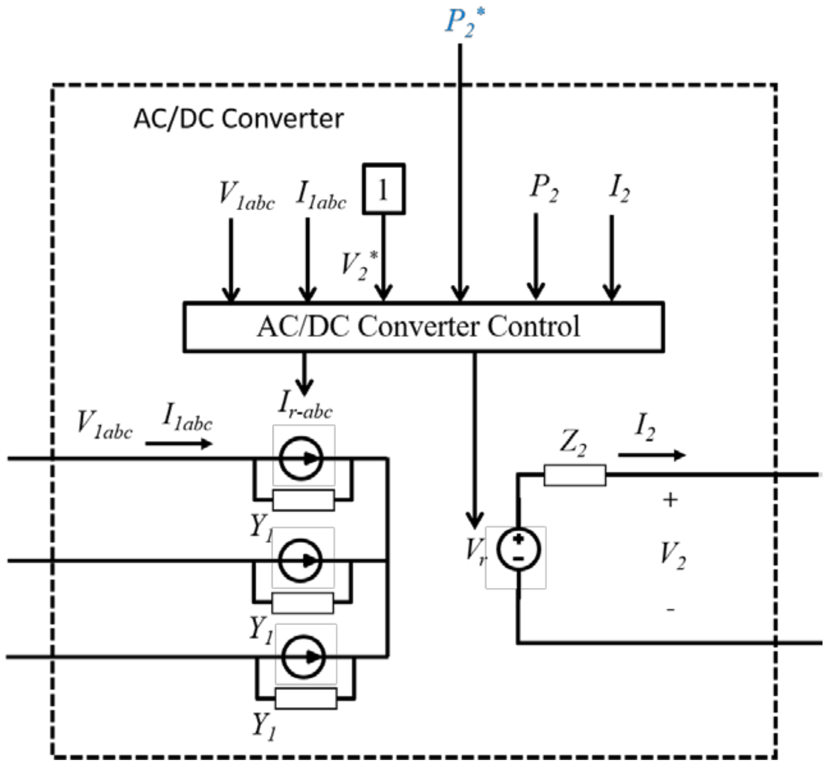

Figure 16 Model for AC-DC converter

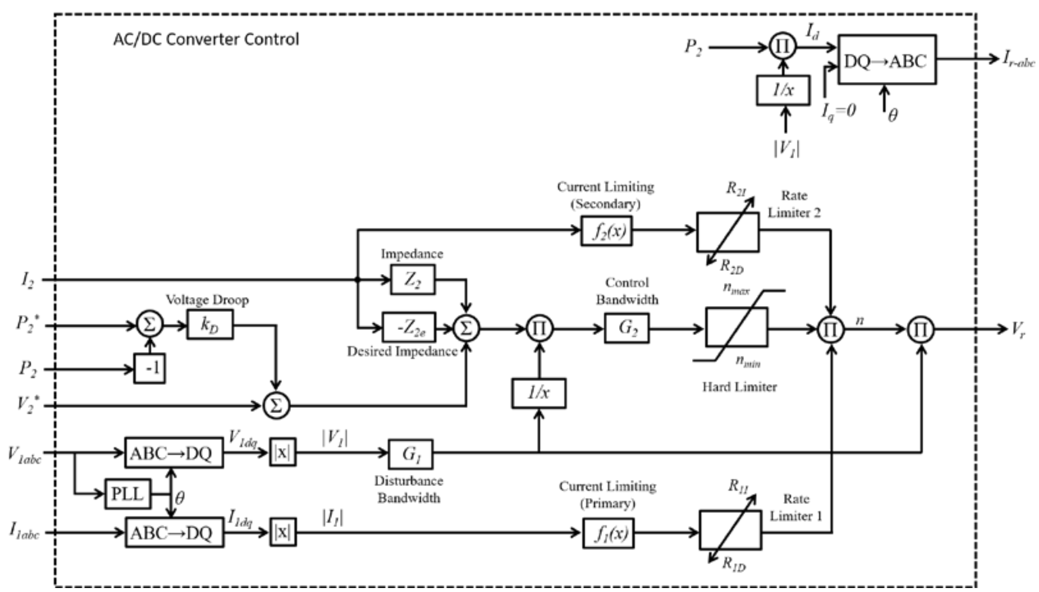

Figure 17 Model for AC-DC converter control

$$Y1(s) = \frac{1}{R1 - Y1} \qquad \textbf{Eq. 7-5}$$

$$Z2(s) = R1 - Z2 + \frac{s(X1 - Z2)}{2\pi f b}$$ **Eq. 7-6**

Z2e(s) = R1-Z2e **Eq. 7-7**

$$Gi(s) = \frac{1}{\left(\frac{s}{2\pi f c - Gi}\right) + 1}$$ **Eq. 7-8**

Table 20 Parameters of AC/DC converter

Block	Parameter	Description	Value
N/A	S_{rated}	Converter apparent power	Variable (MVA)
N/A	P_{rated}	Converter rated power	Variable (MW)
N/A	$V_{1\text{-}rated}$	Converter primary side voltage	Variable (kV)
N/A	$V_{2\text{-}rated}$	Converter secondary side voltage	Variable (kV)
N/A	f_b	Base frequency for purposes of computing reactive components	60 Hz
N/A	$Z_{b\text{-}1}$	Base impedance on primary side	TBD
N/A	$Z_{b\text{-}2}$	Base impedance on secondary side	TBD
Y1	$R_{1\text{-}Y1}$	Converter input admittance resistive component (see Eq. 7-5)	100 pu
Z2	$R_{1\text{-}z2}$	Converter output impedance resistive component (see Eq. 7-6)	0.01 pu
Z2	$X_{1\text{-}z2}$	Converter output impedance reactance component (see Eq. 7-6)	0.05 pu
Voltage Droop	kD	Voltage droop factor	0.1
Desired Impedance	R_{z2e}	Resistive component of desired impedance (see Eq. 7-7)	0 pu
Disturbance bandwidth	$f_{c\text{-}G1}$	Cutoff frequency for primary-side disturbance (see Eq. 7-8)	800 Hz
Control bandwidth	$f_{c\text{-}G2}$	Cutoff frequency for representing control bandwidth (see Eq. 7-8)	250 Hz
Current limiting (primary)	$f_{1(x)}$	Scale factor function for primary side current limiting (see Table 21 and Figure 18)	N/A
Current limiting (secondary)	$f_{2(x)}$	Scale factor function for secondary side current limiting (see Table 21 and Figure 18)	N/A
Rate limiter 1	R_{I1}	Limit for rate of increase	10 pu/s
Rate limiter 1	R_{D1}	Limit for rate of decrease	-100 pu/s
Rate limiter 2	R_{I2}	Limit for rate of increase	10 pu/s
Rate limiter 2	R_{D2}	Limit for rate of decrease	-100 pu/s

Table 21 AC-DC Converter Scale Factor Function for Current Limiting

Current (pu)	Scale Factor
0	1.0
1.1	1.0
1.25	0.0
1.4	0.0

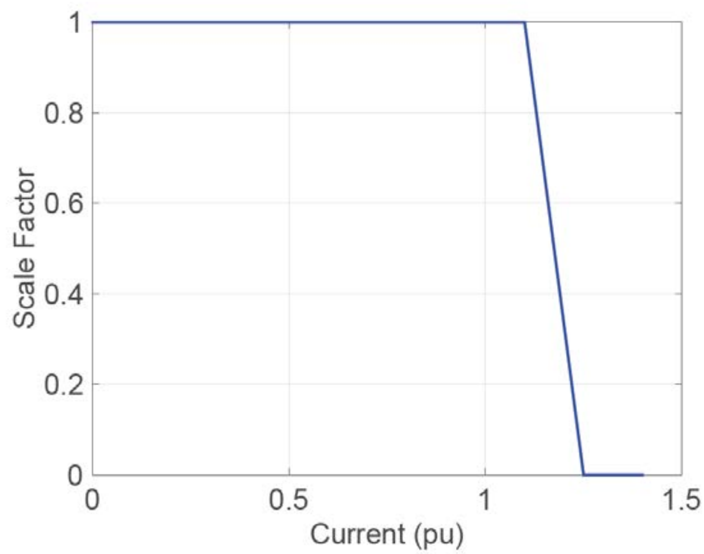

Figure 18 AC-DC Converter Scale Factor Function Current Limiting

7.5 DC - AC Converter

The dc-ac converter model described below is used to model several components in the zonal load centers. The converter model is an average value representation rather than explicitly modeling converter control structure, intended to run on DRTS platforms, for medium bandwidth (MBW) simulation studies.

Figure 19 shows the illustration of dc-dc converter implementation on RTDS. Figure 20 shows the dc-ac converter control stage implementation. The model employs a current injection (I_r) on the primary side and a three phase voltage source (V_{rabc}) on the secondary side. Input and output quantities to the model are entered in per-unit values. The model is based around the concept of an ideal transformer with adjustable turns ratio, n. The controls accept a reference secondary side rms voltage, V_{2abc}, which is biased through the droop characteristic affected by the difference between the reference power P_2* and the actual output power P_2. This voltage reference is further augmented by the term I_{2abc} Z_2 to compensate for the secondary side voltage drop across Z_2. The voltage reference may be further augmented by the term -I_2 Z_{2e} in order to include voltage drop for an emulated impedance, Z_2e. These contributions combine to form the effective voltage reference, V_e. This voltage reference is divided by the primary side voltage, V_1, after applying the filter of $G_{1(s)}$ to this voltage measurement, resulting in the reference turns ratio, n*. Here, $G_{1(s)}$ is intended to represent a restriction in the bandwidth of disturbances on the primary voltage that may propagate through to the secondary side. The filter $G_{2(s)}$, representing the control bandwidth of the converter, is then applied to n*, and the hard limiter is then applied to enforce limits on the minimum and maximum values of the turns ratio. Two other branches are employed to represent the current limiting behavior of the converter. The current limiting functions f1 and f2 provide gains as functions of the primary (I_1) and secondary (I_{2abc}) currents, respectively. These gains are typically unity within the current limits of the converter, and these tend to zero as the current limits are approached. Rate limiters 1 and 2 allow these multiplicative factors to ramp down very quickly, but ramp back to unity more slowly in order to avoid rapid oscillations when current limiting. The result of multiplication with these current-limiting factors is the actual turns ratio, n. This factor is multiplied by the filtered primary side voltage to produce the secondary voltage reference, V_r, which is used to generate a 3 phase voltage reference, V_{rabc} and it is multiplied by the secondary current to provide the primary side current reference, I_r. Generic parameters for the model along with default values for certain elements have been provided in Table 22.

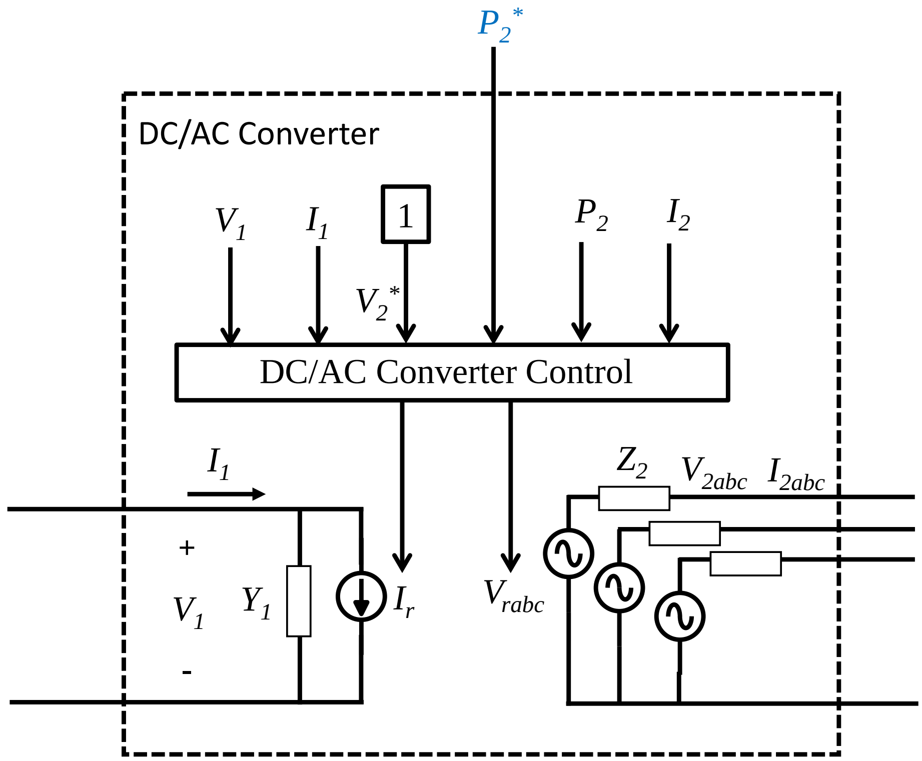

Figure 19 DC-AC Converter Model

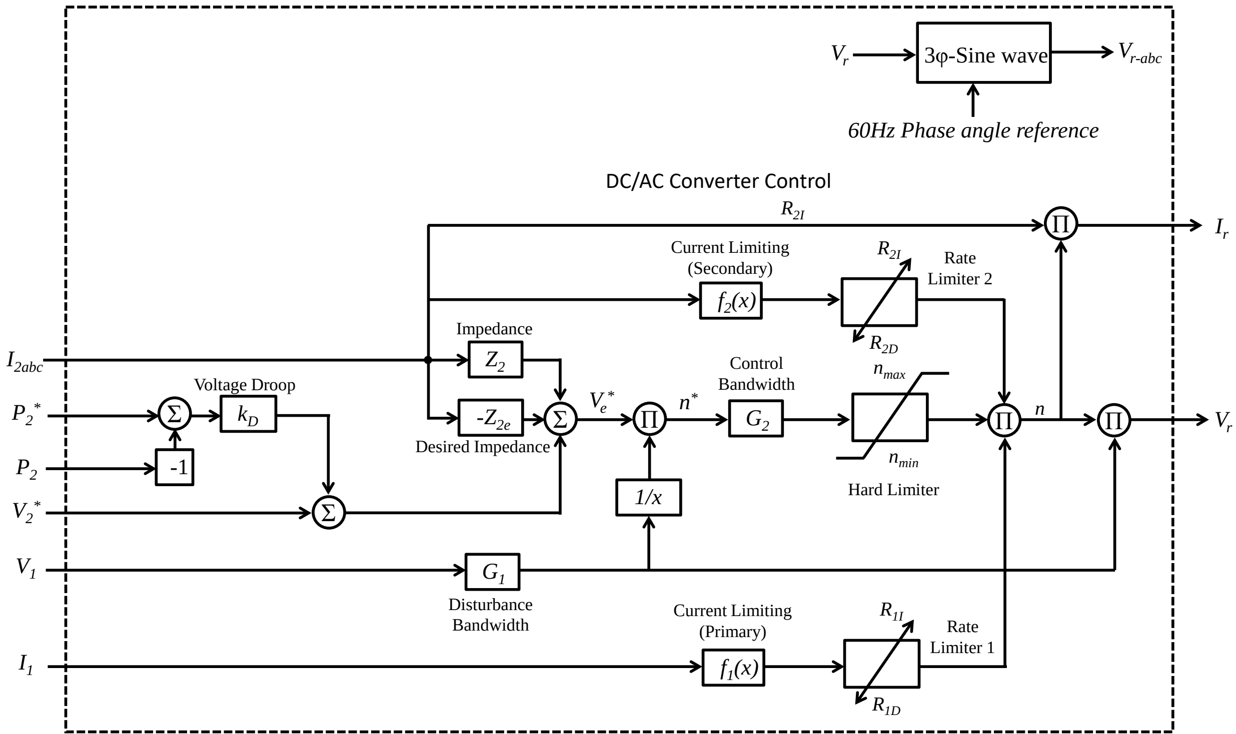

Figure 20 DC-AC converter model control

$$Y1(s) = \frac{1}{R1 - Y1} \qquad \textbf{Eq. 7-9}$$

$$Z2(s) = R1 - Z2 + \frac{s(\,X1 - Z2)}{2\pi f b} \qquad \textbf{Eq. 7-10}$$

$$\text{Z2e(s) = R1-Z2e} \qquad \textbf{Eq. 7-11}$$

$$Gi(s) = \frac{1}{\left(\frac{s}{2\pi f c - Gi}\right) + 1} \qquad \textbf{Eq. 7-12}$$

Table 22 Parameters of DC/AC converter

Block	Parameter	Description	Value
N/A	P_{rated}	Converter rated power	Variable (MW)
N/A	$V_{1\text{-}rated}$	Converter primary side voltage	Variable (kV)
N/A	$V_{2\text{-}rated}$	Converter secondary side voltage	0.450 (kV)
N/A	f_b	Base frequency for purposes of computing reactive components	60 Hz
N/A	$Z_{b\text{-}1}$	Base impedance on primary side	TBD
N/A	$Z_{b\text{-}2}$	Base impedance on secondary side	TBD

Y1	$R_{1\text{-}Y1}$	Converter input admittance resistive component (see Eq. 7-9)	100 pu
Z2	$R_{1\text{-}z2}$	Converter output impedance resistive component (see Eq. 7-10)	0.01 pu
Z2	$X_{1\text{-}z2}$	Converter output impedance reactance component (see Eq. 7-10)	0.05 pu
Voltage Droop	kD	Voltage droop factor	0.1
Desired Impedance	R_{z2e}	Resistive component of desired impedance (see Eq. 7-11)	0 pu
Disturbance bandwidth	$f_{c\text{-}G1}$	Cutoff frequency for primary-side disturbance (see Eq. 7-12)	800 Hz
Control bandwidth	$f_{c\text{-}G2}$	Cutoff frequency for representing control bandwidth (see Eq. 7-12)	250 Hz
Current limiting (primary)	$f_{1(x)}$	Scale factor function for primary side current limiting (see Table 23 and Figure 21)	N/A
Current limiting (secondary)	$f_{2(x)}$	Scale factor function for secondary side current limiting (see Table 23 and Figure 21)	N/A
Rate limiter 1	R_{I1}	Limit for rate of increase	10 pu/s
Rate limiter 1	R_{D1}	Limit for rate of decrease	-100 pu/s
Rate limiter 2	R_{I2}	Limit for rate of increase	10 pu/s
Rate limiter 2	R_{D2}	Limit for rate of decrease	-100 pu/s

Table 23 DC-AC Converter Scale Factor Function for Current Limiting

Current (pu)	Scale Factor
0	1.0
1.1	1.0
1.25	0.0
1.4	0.0

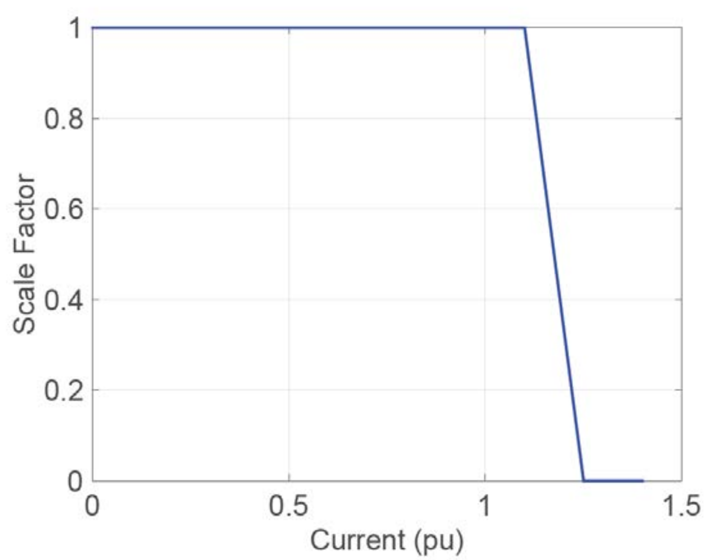

Figure 21 DC-AC Converter Scale Factor Function Current Limiting

7.6 PMM

Figure 22 shows the simplified implementation of PMM. The PMMs are represented as current sinks at MVDC bus. The ship speed can be dialed in which can be translated to power draw at MVDC bus using data provided in Table 24 and Table 25 which provide the motor speed-power curve as well as motor efficiency curve.

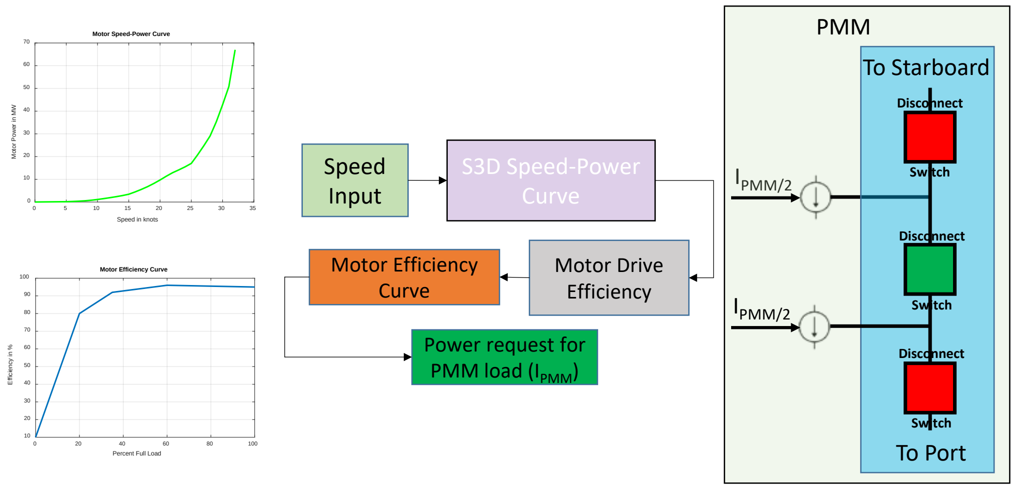

Figure 22 Simplified PMM implementation

Table 24. PMM motor speed-power curve

Speed (knots)	Power (kW)	Speed (knots)	Power (kW)
0	10	19	8,157
5	138	20	9,698
6	241	21	11,359
7	372	22	12,894
8	534	23	14,151
9	794	24	15,482
10	1,121	25	17,004
11	1,502	26	20,755
12	1,918	27	24,780
13	2,359	28	29,074
14	2,851	29	35,362
15	3,432	30	42,840
16	4,434	31	50,811
17	5,543	32	67,000
18	6,760		

Table 25. PMM motor efficiency curve

% Load	Efficiency (%)
0	10
20	80
35	92
60	96
100	95

7.7 HRRL

The example HRRL implementation module draws power equally through both port and starboard bus. The HRRL load is primarily powered through the hybrid energy storage system and control scheme can be implemented to charge the storage system. Figure 23 shows an example HRRL 1 implementation. The module consists of two energy storage elements, an energy dense unit (ESa) that is charged from the MVDC bus that in turn is used to charge the power dense energy storage unit (ESb) which provides power to the HRRL load. The Power/current request for Esa is repernseted through two current sinks on the MVDC bus in zone 2 where in each sink draws half of the total demand. Depending on the switch configuration in the system, the HRRL system can be charged by either port or starboard or both bus.

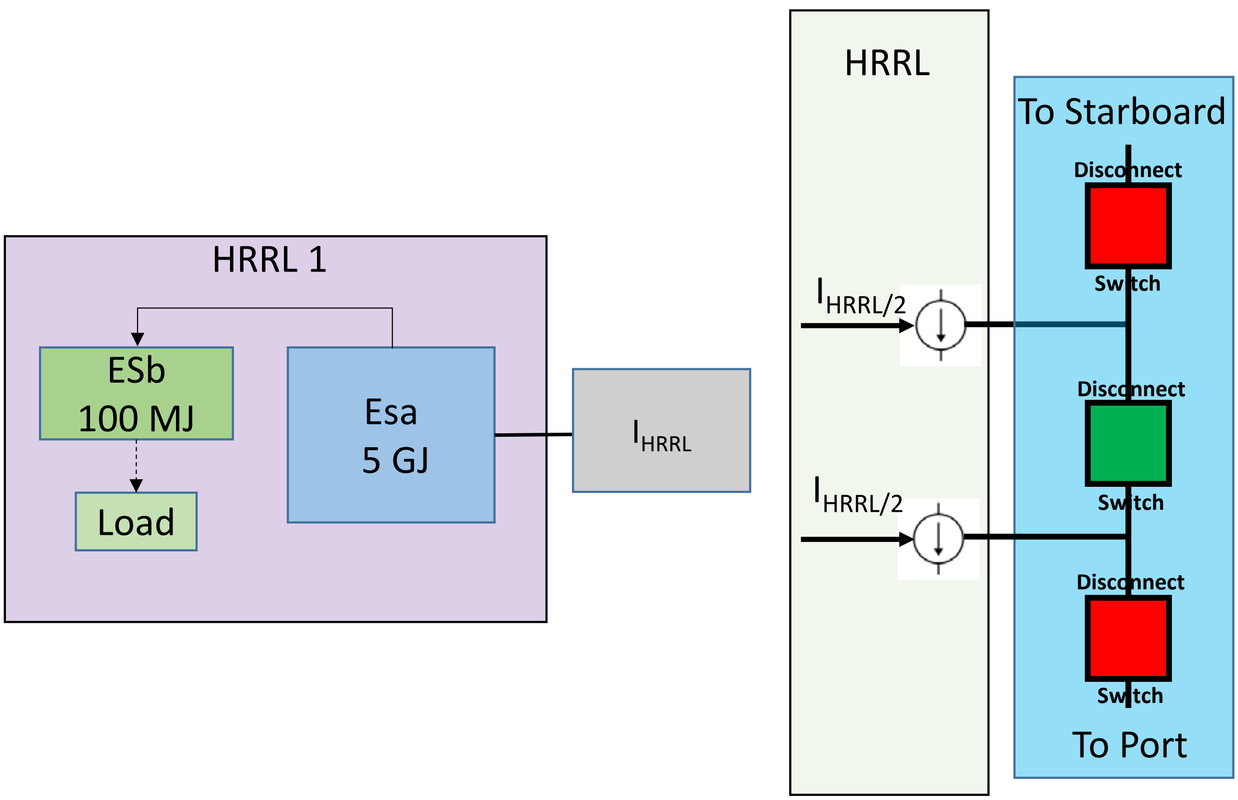

Figure 23 HRRL 1 implementation in RTDS

Table 26. HRRL 1 module parameters

Parameter	Value
HRRL 1 interface converter	20 MW
Energy storage 1	5 GJ
Energy storage 2	100 MJ
HRRL load power demand	20 MW

7.8 Energy Storage Element

For energy storage element, an example of li-ion battery model and its data has been provided in this section. The battery model used is based on Huria/Ceraolo/Gazzarri/Jackey model. The structure of the battery model is shown in Figure 24. The battery model accounts for effects of temperature change on model dynamics as in the internal battery parameters will change based on temperature. The battery model is based on literature presented in [9]. The parameters for the battery are provided in Table 27.

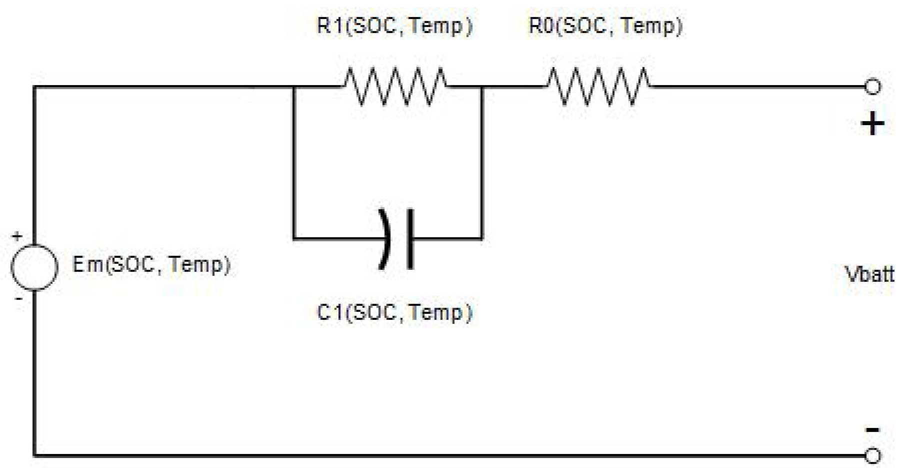

Figure 24 Huria/Ceraolo/Gazzarri/Jackey model structure [9]

Table 27 PCM1A battery parameters

Parameter	Description	Value
Ns	Series cell stack	30
Np	Parallel cell stack	50
Cf	Capacity fade factor	0
initTemp	Initial Ambient Temperature	25 deg C
AH	Individual cell capacity	45 AH
Ct	Heat Capacitance	2040000 (J m-3 K-1)
Rt	Convection Resistance	5.0 (W m-2 K-1)
Tn	Number of entries for temperature	3

SoCn	Number of entries for SoC	7
T	Temperature range	[5.0 20.0 40.0] deg C
SoC	SoC range	[0 20 50 70 80 90 100]
Em	Cell voltrage in order of SoC	[21.65 25.75 26.75 27.625 28.4 29.5 32.5] V
R0	Row order: SOC, column order: Temperature	[0.01169 0.00905 0.008567 0.01099 0.009033 0.00855 0.01139 0.009175 0.008642 0.01076 0.008808 0.008267 0.01068 0.0091 0.008317 0.01128 0.008875 0.008467 0.01156 0.0089 0.008508]
R1	Row order: SOC, column order: Temperature	[0.011 0.00295 0.00133 0.00689 0.00246 0.00124 0.00473 0.00257 0.00133 0.0034 0.00165 0.00105 0.00334 0.00227 0.00143 0.00332 0.0018 0.00107 0.00284 0.00171 0.00103]
C1	Row order: SOC, column order: Temperature	[1.88e+003 1.29e+004 3.07e+004 4.84e+003 1.84e+004 3.34e+004 2.32e+004 4.06e+004 4.74e+004 1.11e+004 1.9e+004 2.68e+004 1.81e+004 3.31e+004 4.81e+004 1.24e+004 1.88e+004 2.7e+004 9.22e+003 2.33e+004 3.03e+004]C1